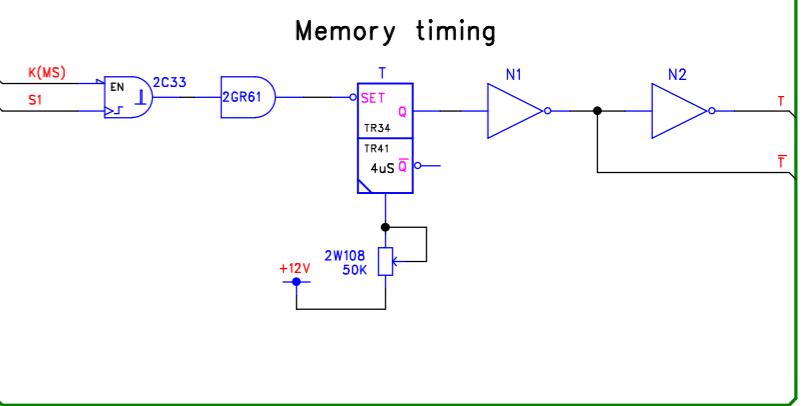
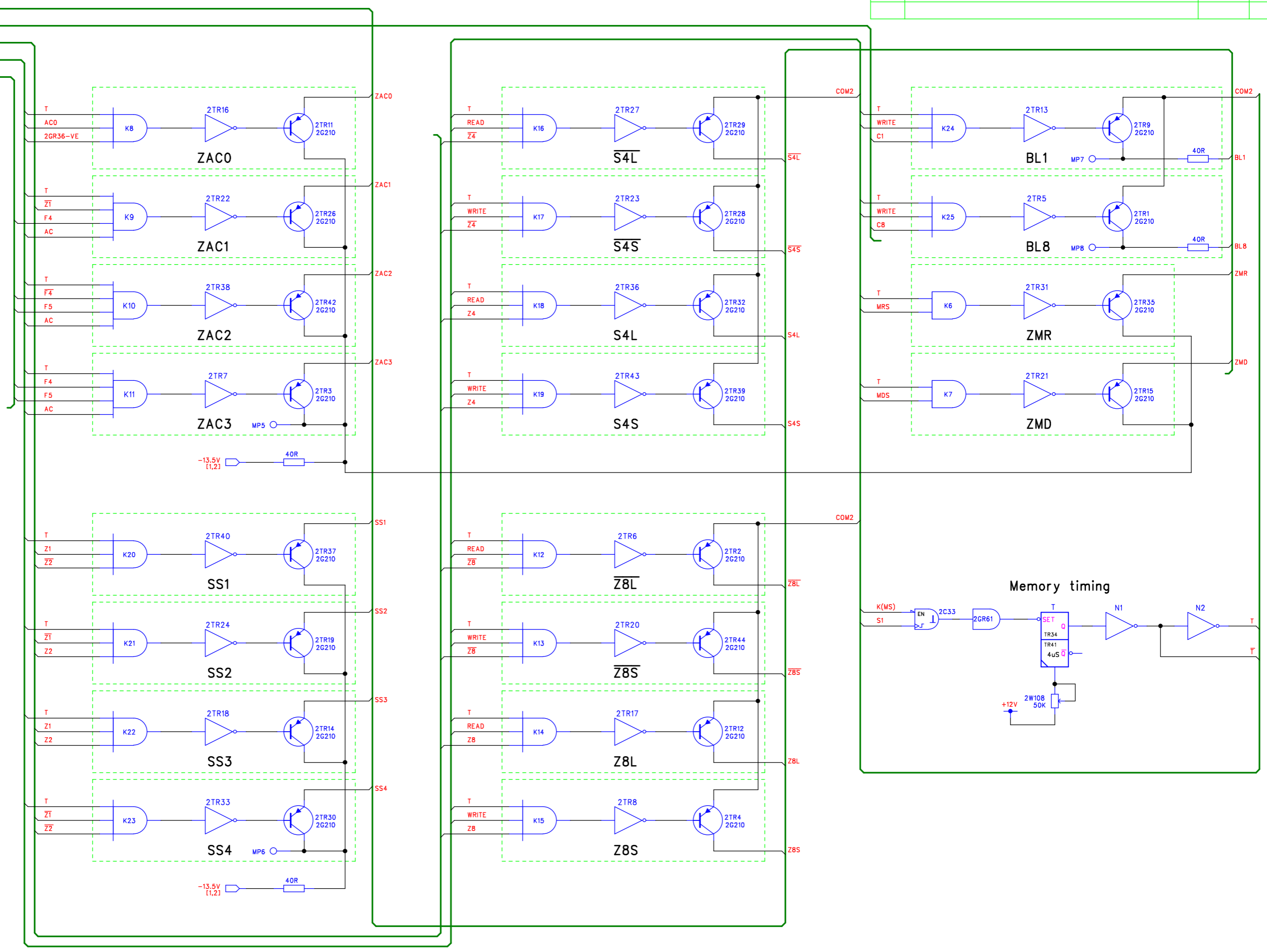


CORE-BUSS [1]
 C-BUSS [1,7,8,14]
 Z-COUNTER [3,4,5,6]
 CONTROL [1,3,4,5,6,7,8,9,10,11,12,14,15,16]
 FUNCTIONS [3,4,5,6,7,8,9,10,11,12,15]

RevNo	Revision note	Date	By	Checked
-	-	-	-	-



Negative logic referenced to 0V - Logical 1 = -12v, logical 0 = 0v



DM Associates
 33, Northbrook Road
 Aldershot, Hampshire. GU11 3HE
 Email: mike@soemtron.org
 www.soemtron.org

© 2021 Mike Hatch. (www.soemtron.org)

Pcb Dwg # =

Name	Date
Drawn MD Hatch	3/02/2021
Checked -	-

Scale	Nts
Sheet 2	2
Next Sheet	3
Drawing Number	

Title	Issue
Soemtron ETR 222 Calculator #2 - Core Memory Drivers Logic Diagram	A