



**AUSTRALIAN ATOMIC ENERGY COMMISSION  
RESEARCH ESTABLISHMENT  
LUCAS HEIGHTS**

**A COMPUTER-TO-COMPUTER DATA LINK FOR A PDP7 AND PDP15**

by

**L.E. TIGHE**

**December 1972**

ISBN 0 642 99523 0



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ABSTRACT

Two adjacent computers are linked so that the peripheral devices connected to each become available to both. The link is arranged so that one computer is master and the other is slave.

National Library of Australia card number and ISBN 0 642 99523 0

The following descriptors have been selected from the INIS Thesaurus to describe the subject content of this report for information retrieval purposes. For further details please refer to IAEA-INIS-12 (INIS: Manual for Indexing) and IAEA-INIS-13 (INIS: Thesaurus) published in Vienna by the International Atomic Energy Agency.

**DATA PROCESSING; DATA TRANSMISSION; INTERFACES; PDP COMPUTERS;  
PROGRAMMING**

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## 1. INTRODUCTION

The AAEC 3 MeV accelerator facility includes two computers for data collection and experiment control. One of the computers, the PDP7, has amongst its peripherals a fast paper tape reader and a fast paper tape punch. Both these devices are essential for the efficient operation of a computer which requires frequent program changes and outputs a large amount of data. The other computer, the PDP15, lacks these devices and has only the very slow ASR33 console for input and output. An alternative to buying a fast paper tape reader, punch and interfacing for the PDP15 was to establish a data link between the PDP7 and the PDP15 so that the input and output devices could be shared.

The proximity of the two computers, their common purpose and the basic similarity of their design strengthened the argument for a data link. The link is also desirable in the situation where only one computer is being used; the memory of the other then becomes available as extra storage.

## 2. PDP7 COMPUTER

This machine has an 18 bit word 1.75 microsecond cycle time and 8192 words of memory (PDP7 User's Handbook). It has a dual 1024 channel analog-to-digital converter and a cathode ray oscilloscope display. There are four scalers connected plus a general input and output register for setting up and determining the status of an experiment. It has direct memory access for multiscaling (PDP7 Interface and Installation Manual p.29). Finally, it has a fast paper tape reader and punch as well as an ASR33 teletype console.

## 3. PDP15 COMPUTER

This machine has an 18 bit word, 1 microsecond cycle time and 8192 words of memory (PDP15 Systems Reference Manual). It has a 4096 channel analog-to-digital converter and a cathode ray display, both connected to the direct memory access (Tighe 1971). Input and output is through an ASR33 teletype console.

## 4. LINK OPERATION

Two tasks are required of the link. The first is to transfer blocks of data from the memory of one computer into the memory of the other. Secondly, a mode is required, specifically for pulse height analysis, in which an address specified in one computer will cause the contents of that location to be incremented in the other computer.

The PDP7 has one direct memory access channel already used for multiscaling, hence access to further peripherals and the link can only be by program transfer (PDP7 Interface and Installation Manual p.7). On the other

hand a number of devices can be multiplexed for use on the PDP15 direct memory access (PDP15 Systems Interface Manual p.4-9). Direct memory access allows data to be transferred into or out of the computer without interfering with other programmed operations. However, if it is desired that the computer continue to execute a program then the data transfers must be compatible with this program.

Since the PDP7 can only transfer data by program control and the PDP15 has direct memory access available, the link was designed so that the PDP7 is master and the PDP15 is slave, as illustrated in block form in Figure 1. The PDP7 as master must contain a program to handle link transfers and transfer data to or from the PDP15 irrespective of the state of that computer. The PDP15 as slave must call upon the PDP7 to execute data transfers initiated from within itself. Table 1 shows the program requirement.

Because no program is required in the PDP15 for PDP7 initiated transfers, all program loading for both computers can be done using the fast paper tape reader on the PDP7.

TABLE 1 SUBROUTINES FOR LINK TRANSFERS

DATA TO	DATA FROM	INITIATED BY	PDP7 SUBROUTINE	PDP15 SUBROUTINE
PDP7	PDP15	PDP7	TRANSIN	NIL
PDP15	PDP7	PDP7	TRANSOUT	NIL
PDP7	PDP15	PDP15	TRANSIN	CALLOUT
PDP15	PDP7	PDP15	TRANSOUT	CALLIN

## 5. PROGRAMMING FOR LINK TRANSFERS

All transfers are made on the basis of a request from one computer and an acknowledge from the other. This means that link transfers are asynchronous. Requests are in the form of interrupts and acknowledgements are flags which can be tested by program. Table 2 sets out the instructions from the PDP7 which control the link.

### 5.1 PDP15 Request Flag

This flag is set by the PDP15 and interrupts the PDP7 program. The purpose is to cause the PDP7 to transfer data into or out of the PDP15 according to its requirements.

### 5.2 Address Register

This register is loaded from the PDP7 Accumulator and is the address in



TABLE 2 PDP7 LINK INSTRUCTIONS

70 6201	SKIP	PDP15 REQUEST FLAG
70 6202	CLEAR	
70 6204	ENABLE	
70 6301	DISABLE	
70 6306		LOAD ADDRESS REGISTER
70 6401	SKIP	DATA CHANNEL FLAG
70 6402	CLEAR	
70 6404	ENABLE	
70 6501	DISABLE	
70 6502		REQUEST WORD FROM PDP15
70 6504		LOAD PDP7 ACCUMULATOR FROM LINK
70 6601		SET PDP7 ACKNOWLEDGE FLAG
70 6602		TRANSFER WORD TO PDP15
70 6604		INCREMENT PDP15 MEMORY

the PDP15 memory which is to be loaded or read by direct memory access.

### 5.3 Data Channel Flag

This flag is set when a direct memory access transfer to or from the PDP15 has been completed. The direct memory access is activated by one of the instructions described in 5.4 to 5.6.

#### 5.4 Request Word From PDP15 (70 6502)

This instruction requests that the contents of the location specified in the address register be loaded from the PDP15 into the link register. When this has been done the data channel flag is set and the PDP7 loads the contents of the link register into its accumulator using the instruction 70 6504.

#### 5.5 Transfer Word to PDP15 (70 6602)

This instruction requests that the contents of the link register be loaded into the PDP15 at the location specified in the address register. The same instruction loads the link register from the PDP7 accumulator. At the completion of the transfer the data channel flag is set.

#### 5.6 Increment PDP15 Memory (70 6604)

This instruction increments the location in the PDP15, specified in the address register. On completion, the data channel flag is set.

**Note:** At the completion of each of the above three instructions the address register is automatically incremented. This results in ease of programming for transfers of blocks of data.

Table 3 sets out the instructions which access the PDP7 from the PDP15.

TABLE 3 PDP15 LINK INSTRUCTIONS

70 2201	SKIP ON PDP7 ACKNOWLEDGE FLAG
70 2202	SET PDP15 REQUEST FLAG
70 2204	CLEAR AND ENABLE PDP7 ACKNOWLEDGE FLAG

#### 5.7 PDP7 Acknowledge Flag

This flag is set by the PDP7 when it has completed the transfer of data requested by the PDP15. It causes an interrupt to the PDP15 program.

#### 5.8 Data Transfer Programs

The use of the link control instructions is demonstrated in the two program segments in the Appendix. The routine, TRANSOUT in the PDP7 is called by the main program when data is to be transferred to the PDP15. The address of the data in the PDP7, the address of the destination in the PDP15 and the number of words to be transferred are specified.

The routine TRANSIN in the PDP7 is called by the main program when data is to be transferred from the PDP15 to the PDP7. Again starting addresses and block size are specified.

## 6. LINK INTERFACE

This consists of two parts. The PDP7 being a negative bus machine

(logical zero = ground, logical one = - 3 volts) requires a positive bus converter so that its data levels are compatible with the positive bus (logical zero = ground, logical one = + 3 volts) on the PDP15. The positive bus converter is installed in the PDP7 cabinet and cables extend this bus to the PDP15 which contains the link handler. Symbols used in the circuit diagrams are tabulated in Figure 2 and symbols nomenclature is shown in Figure 3.

#### 6.1 PDP7 Positive Bus Converter

Figure 4 shows all the PDP7 bus lines with the appropriate level converters. The lines on the bus are input and output, memory buffer, input-output pulses, program interrupt, skip, power clear and read status. Figure 5 shows the cable schedule and Figure 6 shows the layout of cards.

#### 6.2 Link Handler

The data channel multiplexing circuits for the PDP15 appear on the left of Figure 7 and on the right are shown two flip-flops which determine the mode of transfer. The flip-flops set the state of three control lines and the relationships between these states and the transfer modes are shown in Table 4.

TABLE 4 STATE OF THE CONTROL LINES  
TO GIVE THE TRANSFER MODES OF THE PDP15 DATA CHANNEL  
0 REPRESENTS ZERO VOLTS AND 1 REPRESENTS 2.5 VOLTS

TRANSFER MODE	PDP15 CONTROL LINES		
	SINGLE CYCLE	INCREMENT MEMORY	DATA CHANNEL
INTO PDP15	0	1	0
OUT OF PDP15	0	1	1
INCREMENT MEMORY	1	0	0

The lower part of Figure 7 shows all the flags for exhibiting the state of the link. The flags are identified by the skip instructions from the two computers. The device selectors for program control of the link are shown in Figure 8.

Figure 9 illustrates the link data register. This can be loaded by either computer or read by either computer, hence data transfers must only be in one direction at a time. As data transfers are under the control of the master computer at all times the direction of transfer is always known.

The link address register appears in Figure 10. As well as having provision for loading by the PDP7 and reading by the PDP15, it can be incremented. Any access to the PDP15 data channel by the link increments the address register after the transfer is completed.

Figures 11 and 12 show the input-output cable schedule and Figure 13 gives the layout of cards.

#### 7. REFERENCE

Tighe, L.E. (1971) - Pulse Height Analysis Using a PDP15 Computer, AAEC/TM593.

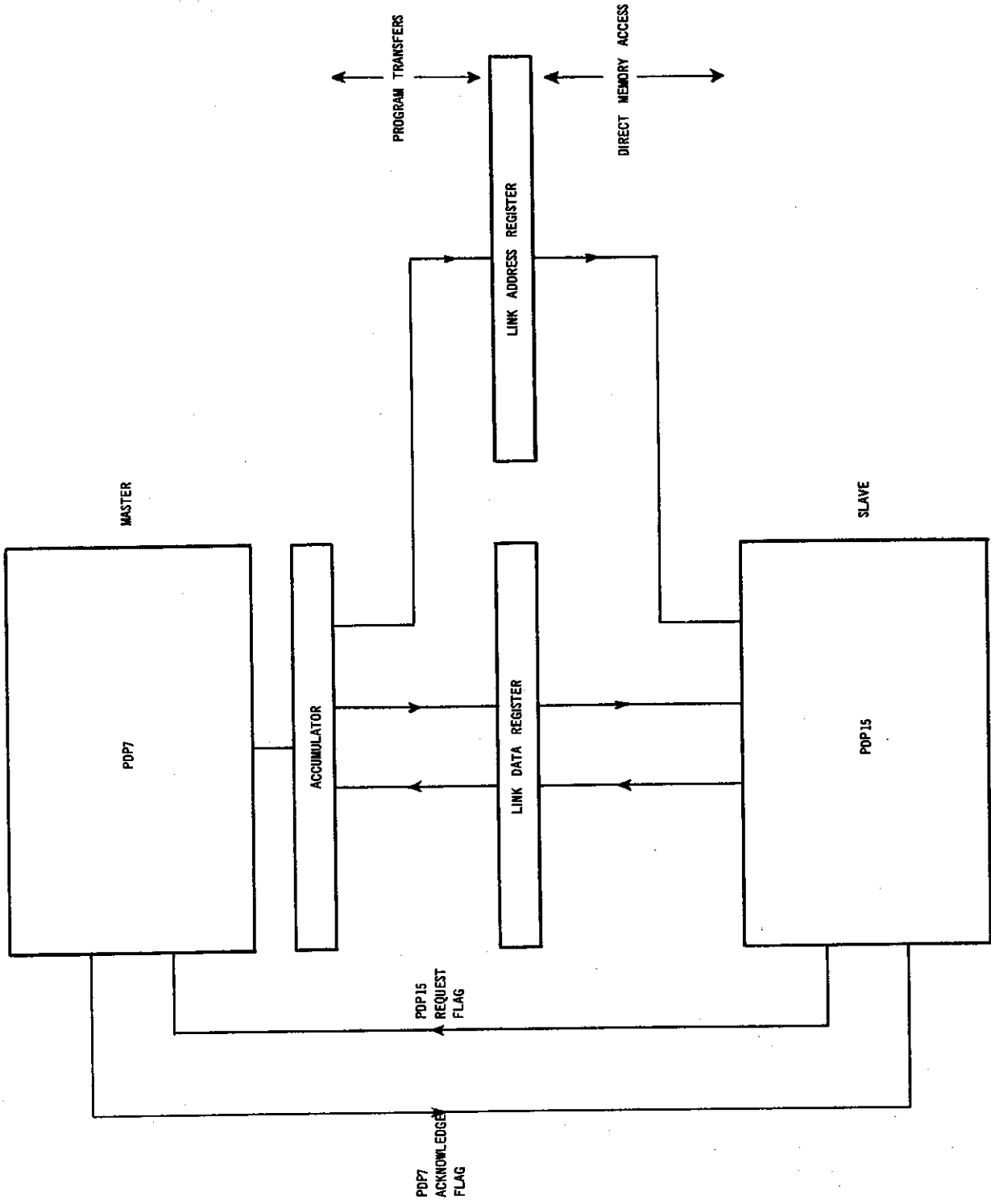
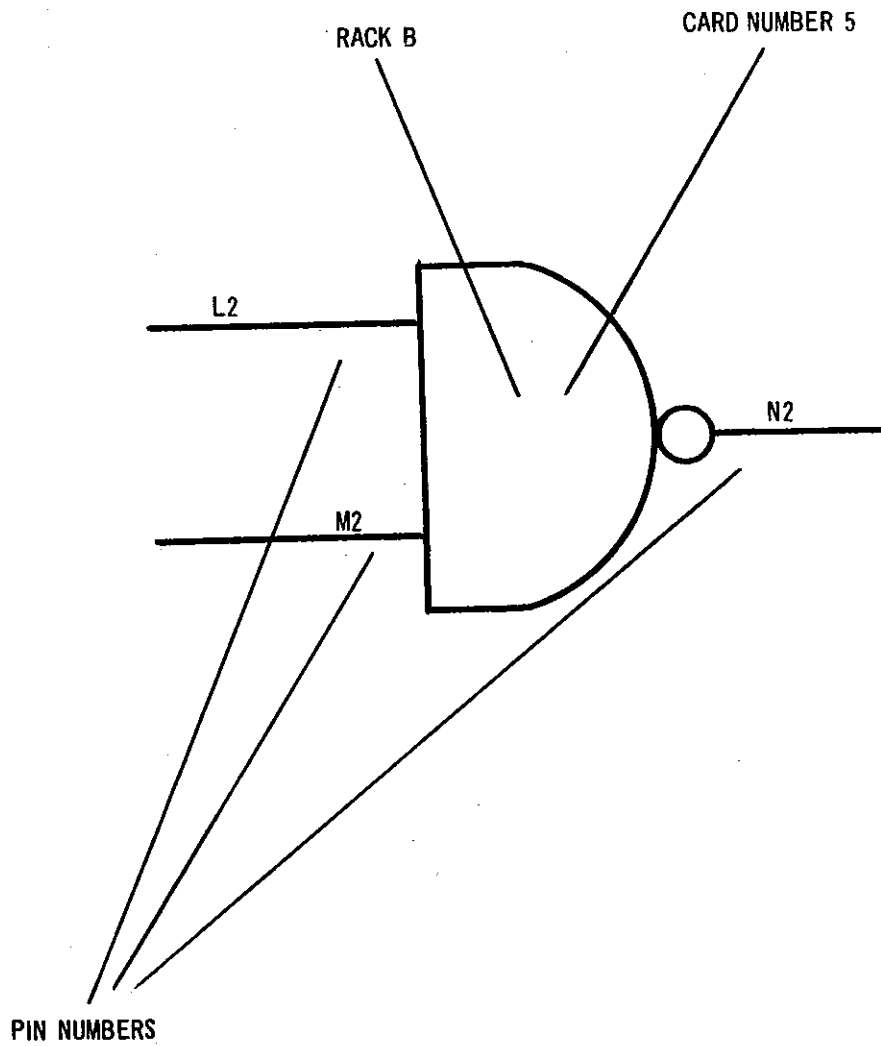


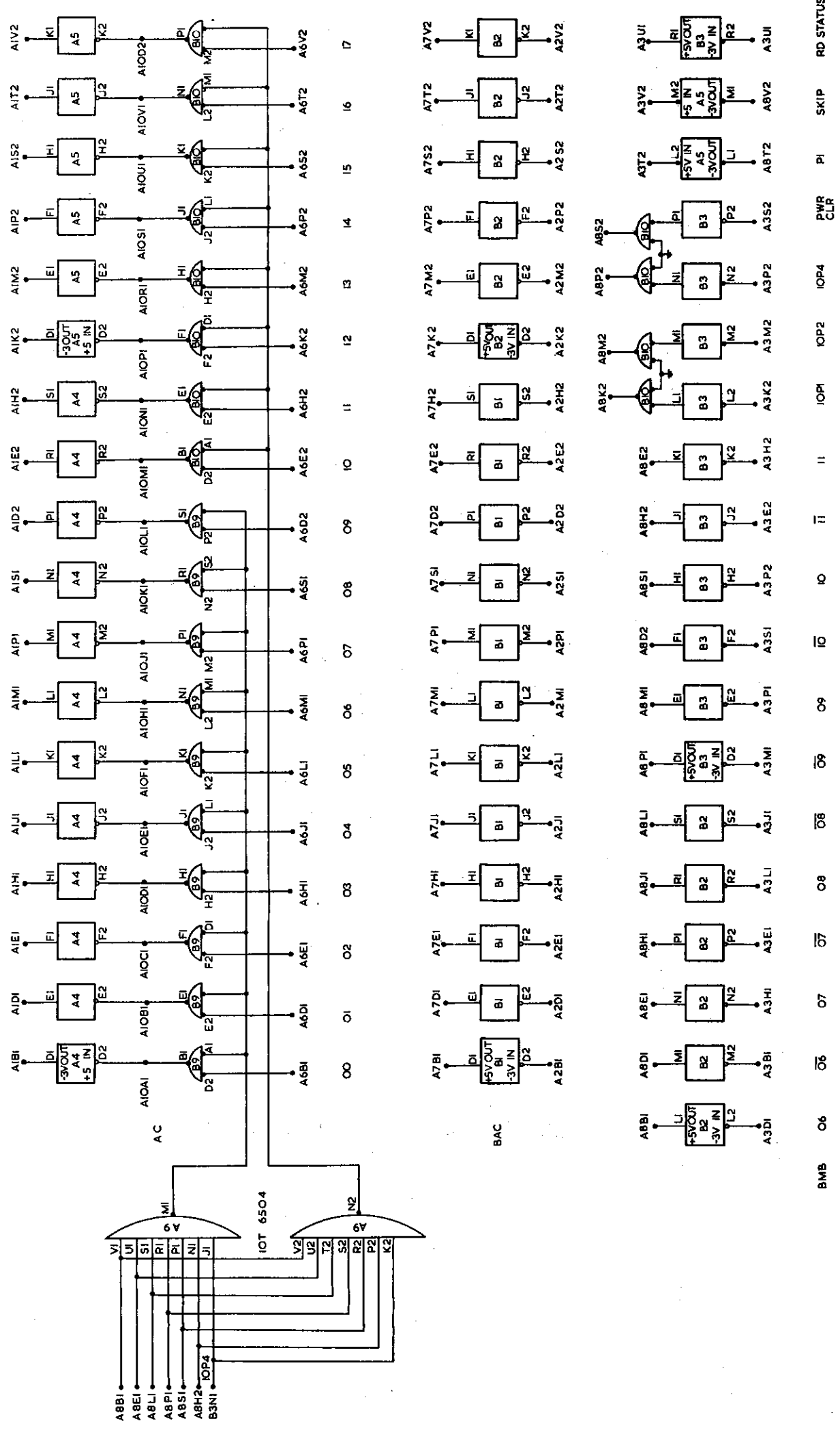
FIGURE 1. PDP7 PDP15 LINK - BLOCK DIAGRAM

<u>SYMBOL</u>	<u>FUNCTION</u>	<u>NAME</u>	<u>REMARKS</u>
	OR-GATE	L623 OR L624	OPEN COLLECTOR OUTPUT 220 OHM DRIVER OR 50 OHM DRIVER
	NAND-GATE	L7400	
	NEGATIVE NOR-GATE		
	NEGATIVE NAND-GATE	L7402	
	NOR-GATE		
	8-INPUT NAND-GATE	L7430	
	ONE-SHOT	L803	ADDITIONAL DELAY WITH EXTERNAL CAPACITOR
	D-TYPE FLIP-FLOP	L7474	

**FIGURE 2. TABLE OF SYMBOLS**



**FIGURE 3. SYMBOL NOMENCLATURE**



**FIGURE 4. PDP7 POSITIVE BUS - LEVEL CONVERTERS**



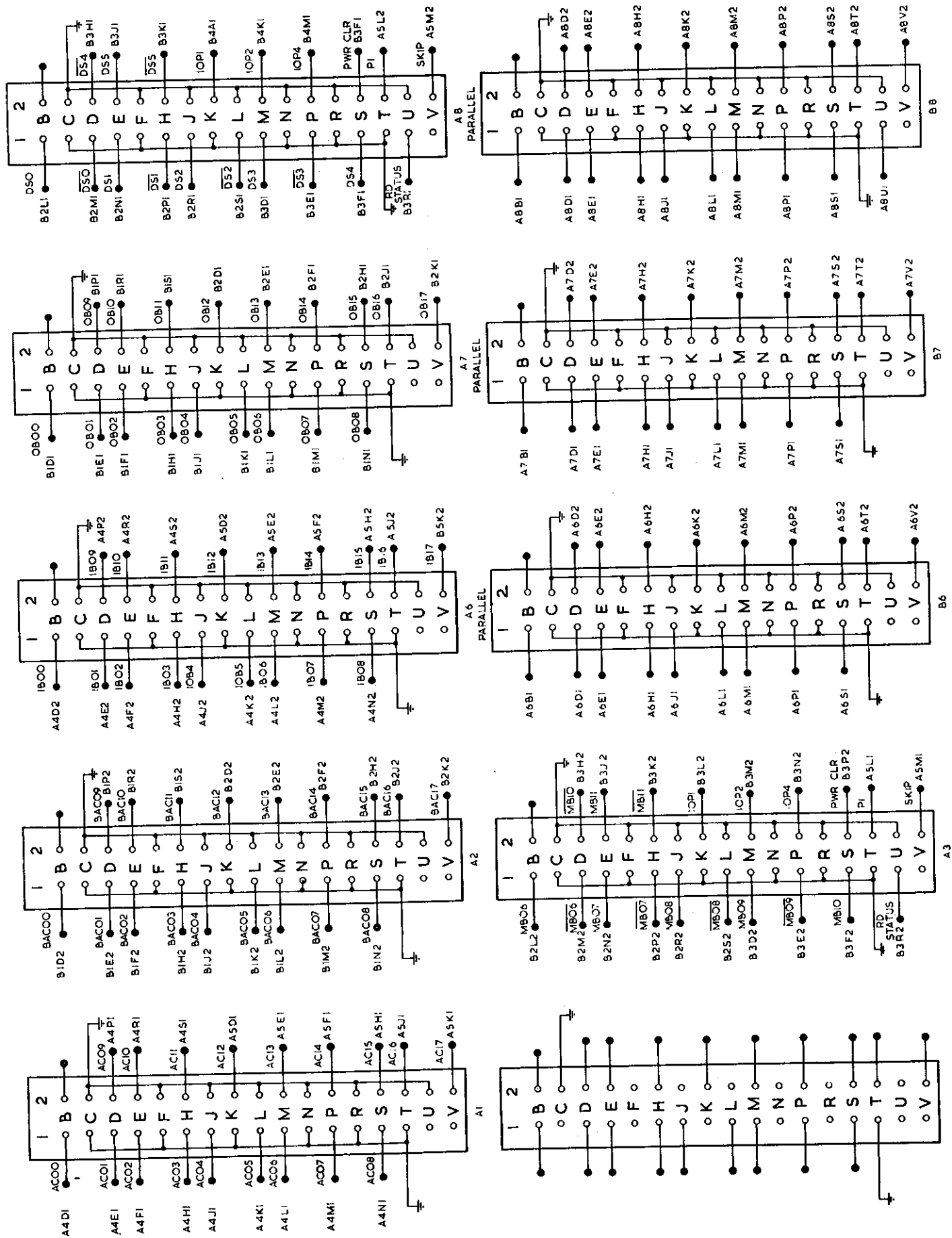


FIGURE 5. PDP7 POSITIVE BUS - INPUT-OUTPUT SCHEDULE

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32			
LO23	LO23	LO23	MO51	MO51	LO23	LO23	LO23																											
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32			
L111	L111	L111			LO23	LO23	LO23																											

FIGURE 6. PDP7 POSITIVE BUS - CARD ALLOCATION SCHEDULE

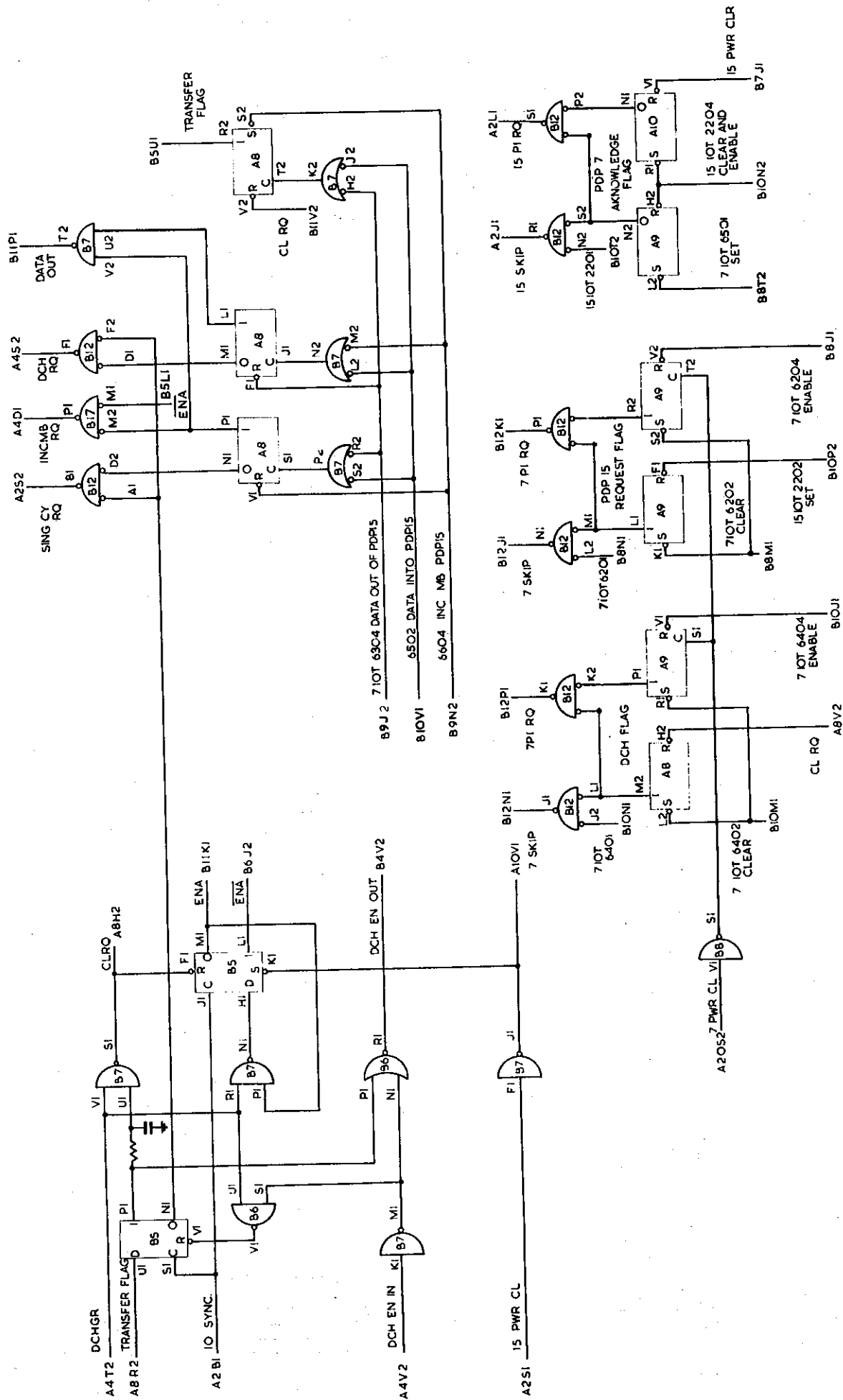


FIGURE 7. PDP7 PDP15 LINK - DATA CHANNEL CONTROL AND FLAGS

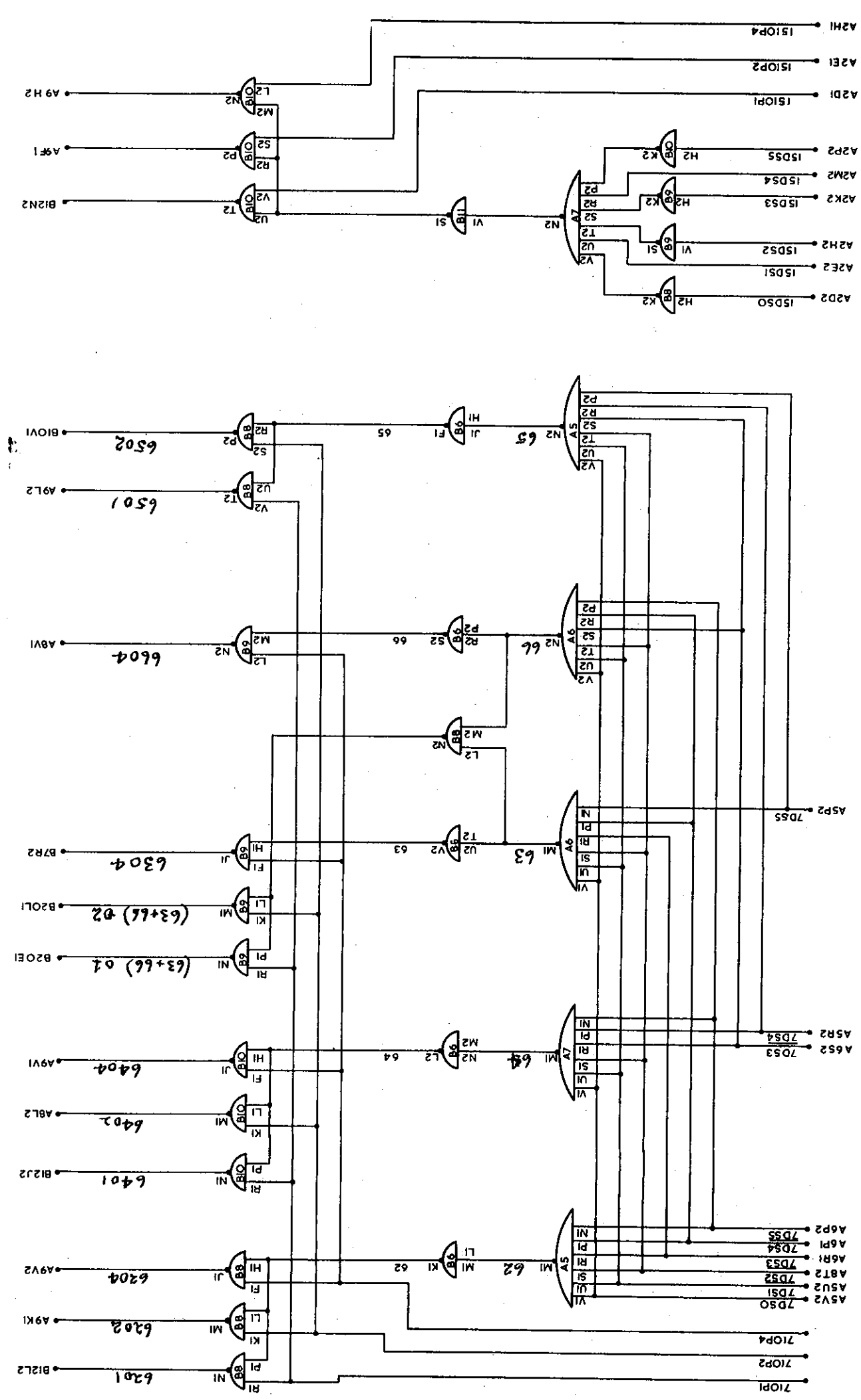


FIGURE 8. PDP7 PDP15 LINK - DEVICE SELECTORS

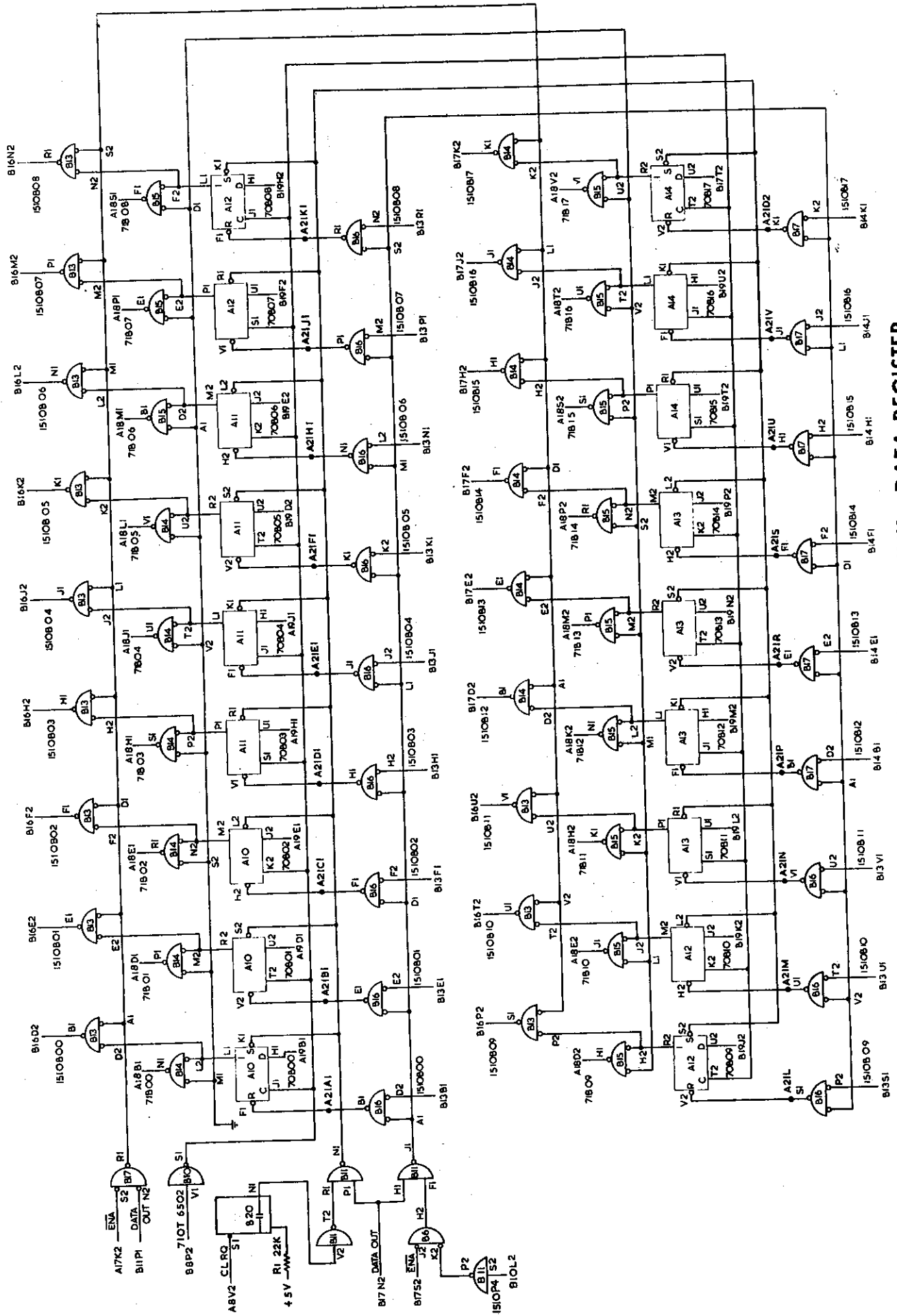


FIGURE 9. PDP7 PDP15 LINK - DATA REGISTER

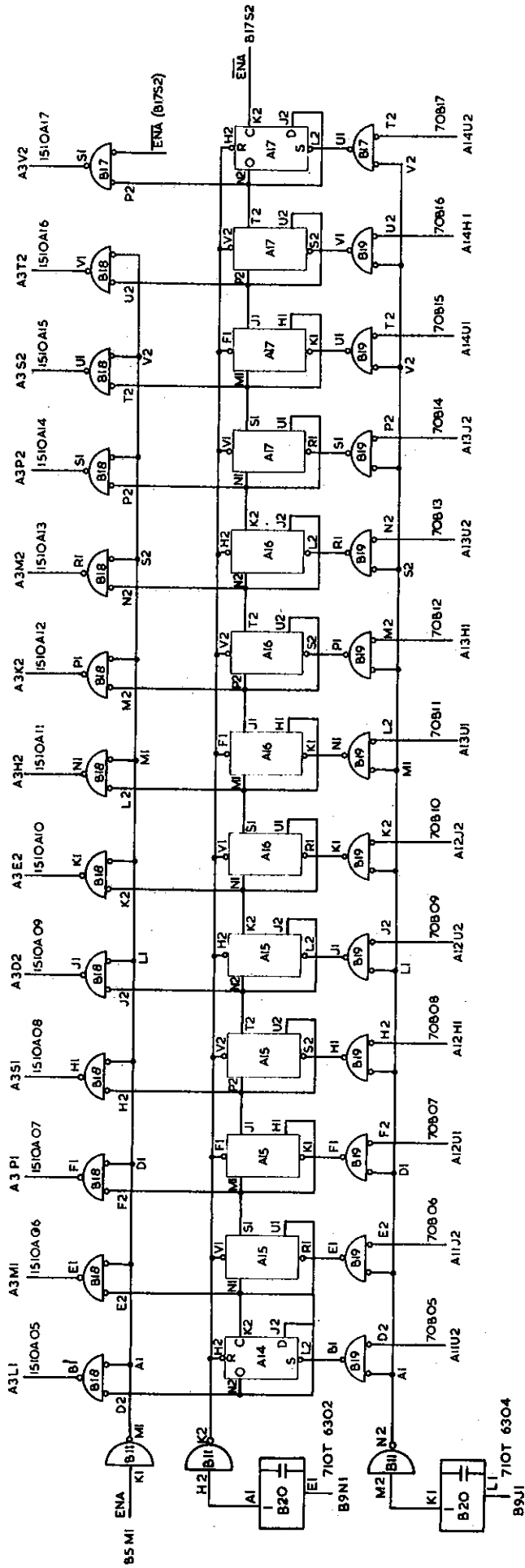


FIGURE 10. PDP7 PDP15 LINK - ADDRESS REGISTER

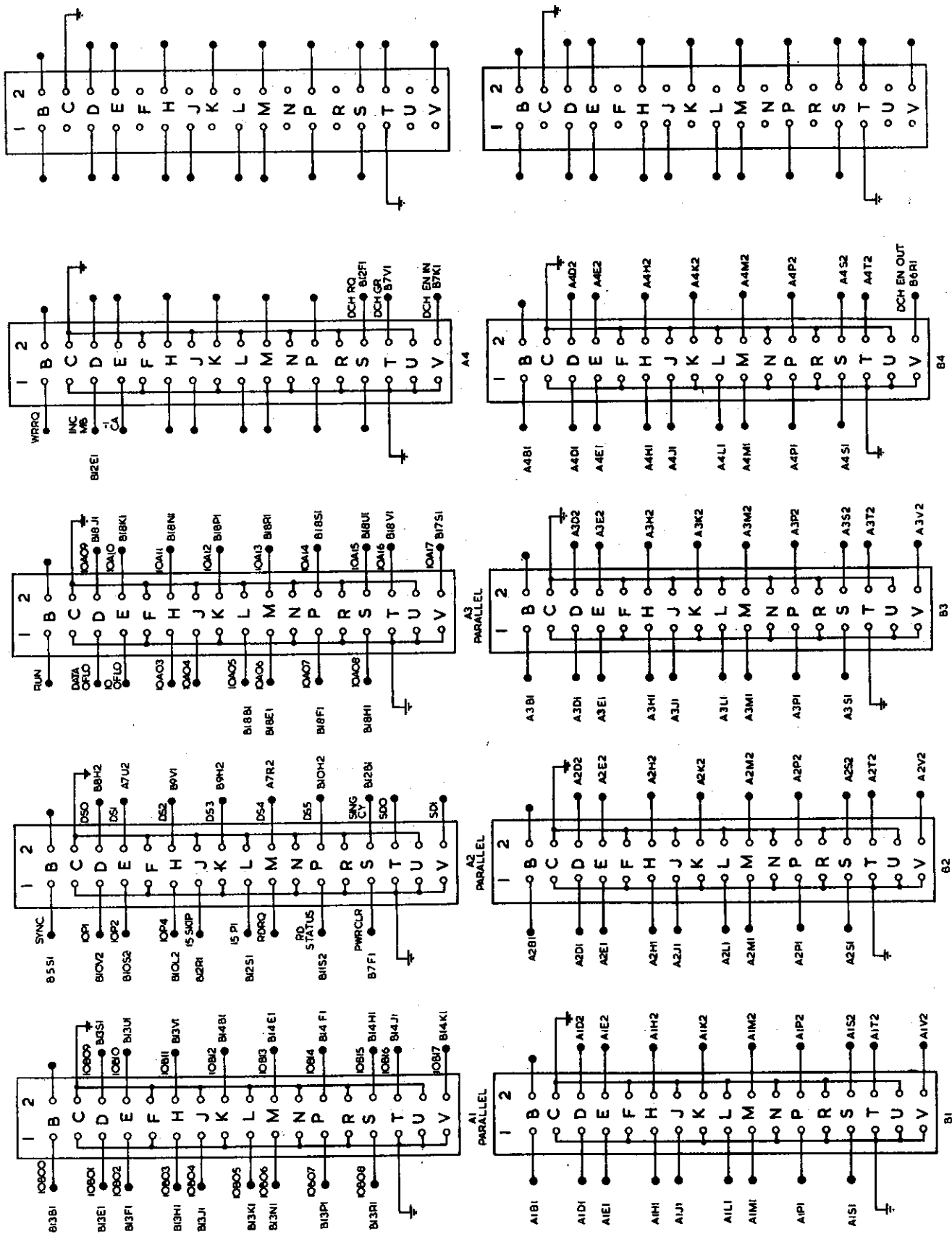


FIGURE 11. PDP7 PDP15 LINK - PDP15 BUS SCHEDULE

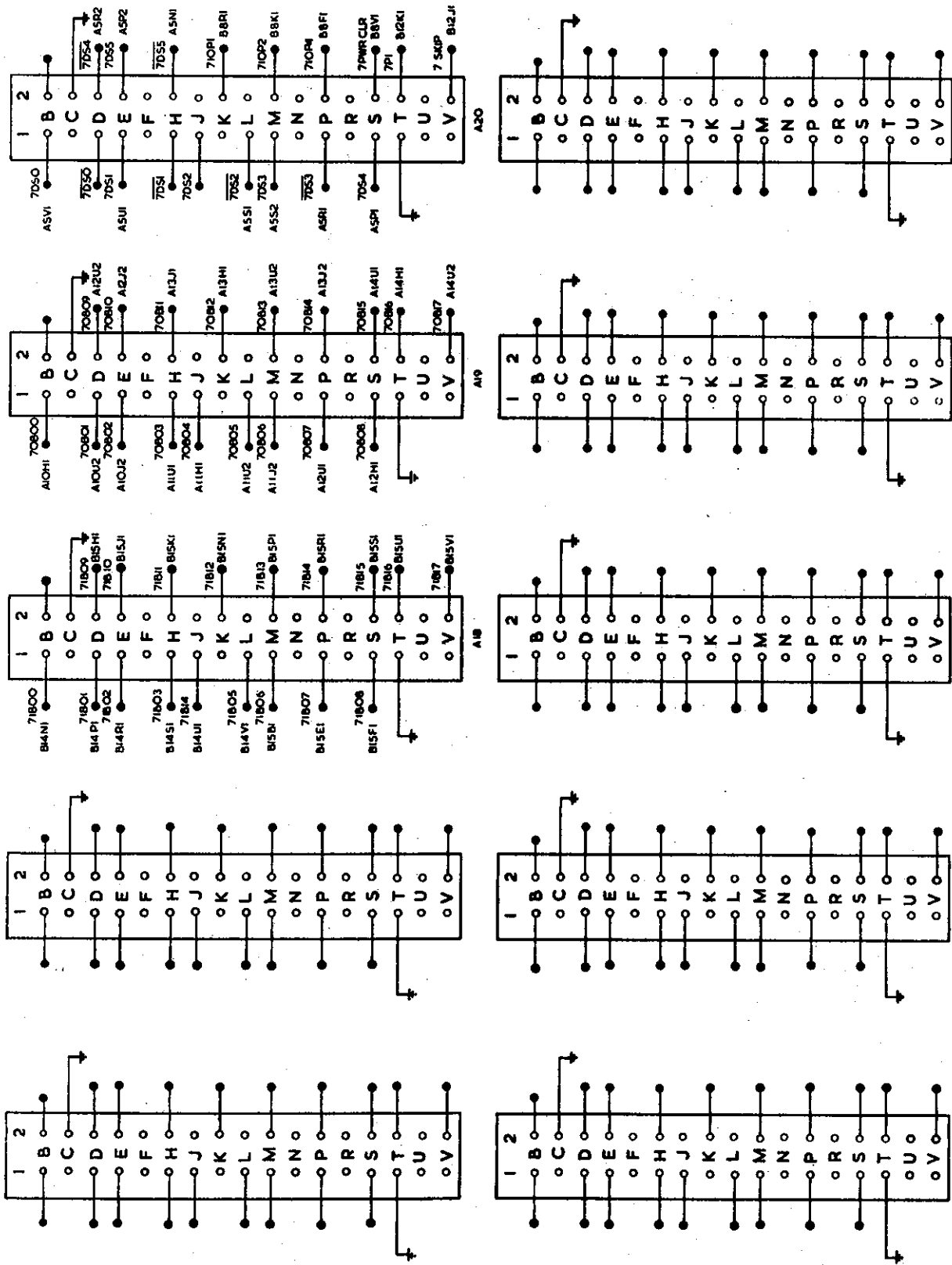


FIGURE 12. PDP7-PDP15 LINK - PDP7 BUS SCHEDULE



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32			
LO23	LO23	LO23	LO23	L7430	L7430	L7430	L7474	L7474	L7474	L7474	L7474	L7474	L7474	L7474	L7474	L7474	L7474	LO23	LO23															
				3-2	3-2	3-2	2-4	2-4	2-1	4-4	4-4	4-4	4-3	5-4	5-4	5-4																		
	PDP-15 BUS IN																PDP-7 BUS																	
LO23	LO23	LO23	LO23	L7474	L7402	L7400	L7400	L7400	L7400	L7400	L623	L623	L623	L623	L623	L623	L623	L623	L623	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32		
				2-2	2-2	2-8	2-1	3-8	3-7	4-3	2-10	4-12	4-12	4-12	4-12	4-12	4-7	5-12	5-12															
				3-5	3-5	3-7	4-1	5-1	5-1	3-1																								
				4-1	4-1																													
	PDP-15 BUS OUT																																	

SHEET NO. - NO. OF ELEMENTS

FIGURE 13. PDP7 PDP15 LINK - CARD ALLOCATION SCHEDULE



APPENDIX

Program Segments Demonstrating Link Control Instructions

(a) TRANSOUT

/ ROUTINE TRANSOUT TRANSFERS DATA BLOCK FROM PDP7 TO PDP15  
/ CALLING SEQUENCE  
/       JMS TRANSOUT  
/       STARTING ADDRESS IN PDP15  
/       STARTING ADDRESS IN PDP7  
/       - (SIZE OF BLOCK)

TRANSOUT, 0

LAC I TRANSOUT  
70 7306                / LOAD ADDRESS REGISTER  
ISZ TRANSOUT  
LAC I TRANSOUT        / GET PDP7 ADDRESS  
DAC TEM  
ISZ TRANSOUT  
LAC I TRANSOUT        / GET SIZE OF BLOCK  
DAC CNTR  
LAC I TEM  
70 6602                / TRANSFER WORD TO PDP15  
70 6401                / SKIP ON DATA CHANNEL FLAG  
JMP   .-1              /WAIT UNTIL TRANSFER COMPLETED  
70 6402                / CLEAR DATA CHANNEL FLAG  
ISZ TEM  
ISZ CNTR               /SKIP WHEN BLOCK TRANSFERRED  
JMP   .-7  
ISZ TRANSOUT         / SET RETURN  
JMP I TRANSOUT        / EXIT

APPENDIX (Cont'd.)

(b) TRANSIN

/ ROUTINE TRANSIN TRANSFERS DATA BLOCK FROM PDP7 TO PDP15

/ CALLING SEQUENCE

/ JMS TRANSIN

/ STARTING ADDRESS IN PDP15

/ STARTING ADDRESS IN PDP7

/ - (SIZE OF BLOCK)

TRANSIN, 0

LAC I TRANSIN

70 6306 / LOAD ADDRESS REGISTER

ISZ TRANSIN

LAC I TRANSIN / GET PDP7 ADDRESS

DAC TEM

ISZ TRANSIN

LAC I TRANSIN / GET SIZE OF BLOCK

DAC CNTR

70 6502 / REQUEST WORD FROM PDP15

70 6401 / SKIP ON DATA CHANNEL FLAG

JMP .-1

70 6402 / CLEAR DATA CHANNEL FLAG

70 6504 / LOAD PDP7 ACCUMULATOR FROM LINK

DAC I TEM

ISZ TEM

ISZ CNTR / SKIP WHEN BLOCK TRANSFERRED

JMP .-7

ISZ TRANSIN / SET RETURN

JMP I TRANSIN / EXIT