

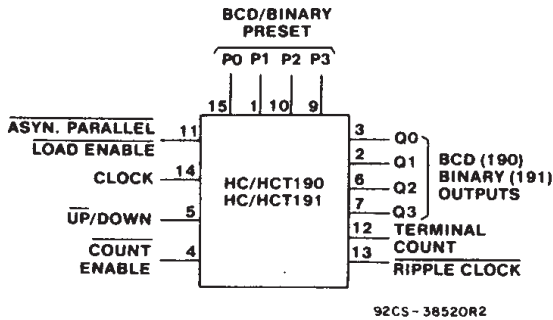
CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191



Data sheet acquired from Harris Semiconductor
SCHS275

High-Speed CMOS Logic

Presettable Synchronous 4-Bit Up/Down Counters



FUNCTIONAL DIAGRAM

CD54/74HC/HCT190 BCD Decade Counter
CD54/74HC/HCT191 Binary Counter

Type Features:

- Synchronous counting and asynchronous loading
- Two outputs for n-bit cascading
- Look-ahead carry for high-speed counting

The RCA-CD54/74HC/HCT190/191 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a Low asynchronous parallel load input (\overline{PL}). Counting occurs when \overline{PL} is high, Count Enable (\overline{CE}) is low, and the Up/Down ($\overline{U/D}$) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

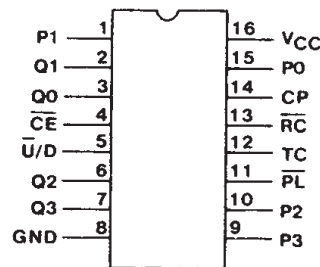
When an overflow or underflow of the counter occurs the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Fig. 6). The TC output also initiates the Ripple Clock (\overline{RC}) output which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Clock output as shown in Fig. 7.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts as shown in state diagrams.

The CD54HC/HCT190 and the CD54HC/HCT191 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT190 and the CD74HC/HCT191 are supplied in a 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT190 and the CD54/74HC/HCT191 are also supplied in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , @ $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V$ Max., $V_{IH} = 2 V$ Min.
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}



92CS-38521

**HC/HCT190, HC/HCT191
TERMINAL ASSIGNMENT**

This data sheet is applicable to the CD54HC190, CD74HC190, CD74HCT190, CD54HC191, and CD54HCT191. The CD54HCT190 was not acquired from Harris Semiconductor. See SCHS192 for information on the CD74HC191 and CD74HCT191.

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

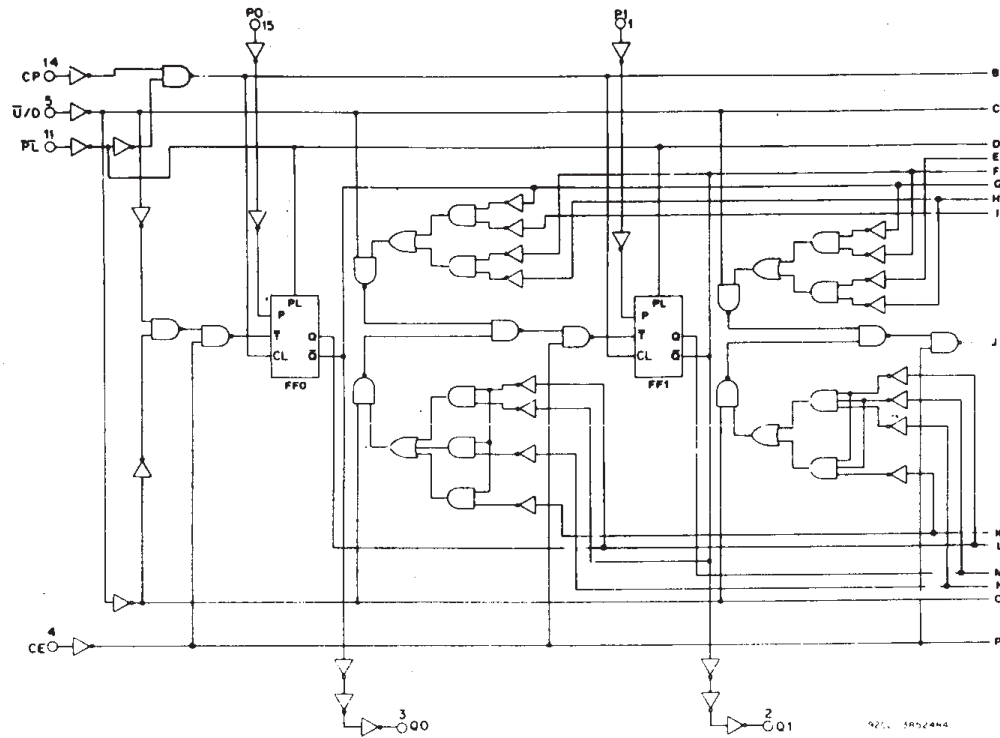


Fig. 1 - Logic diagram for HC/HCT190 (continued on next page).

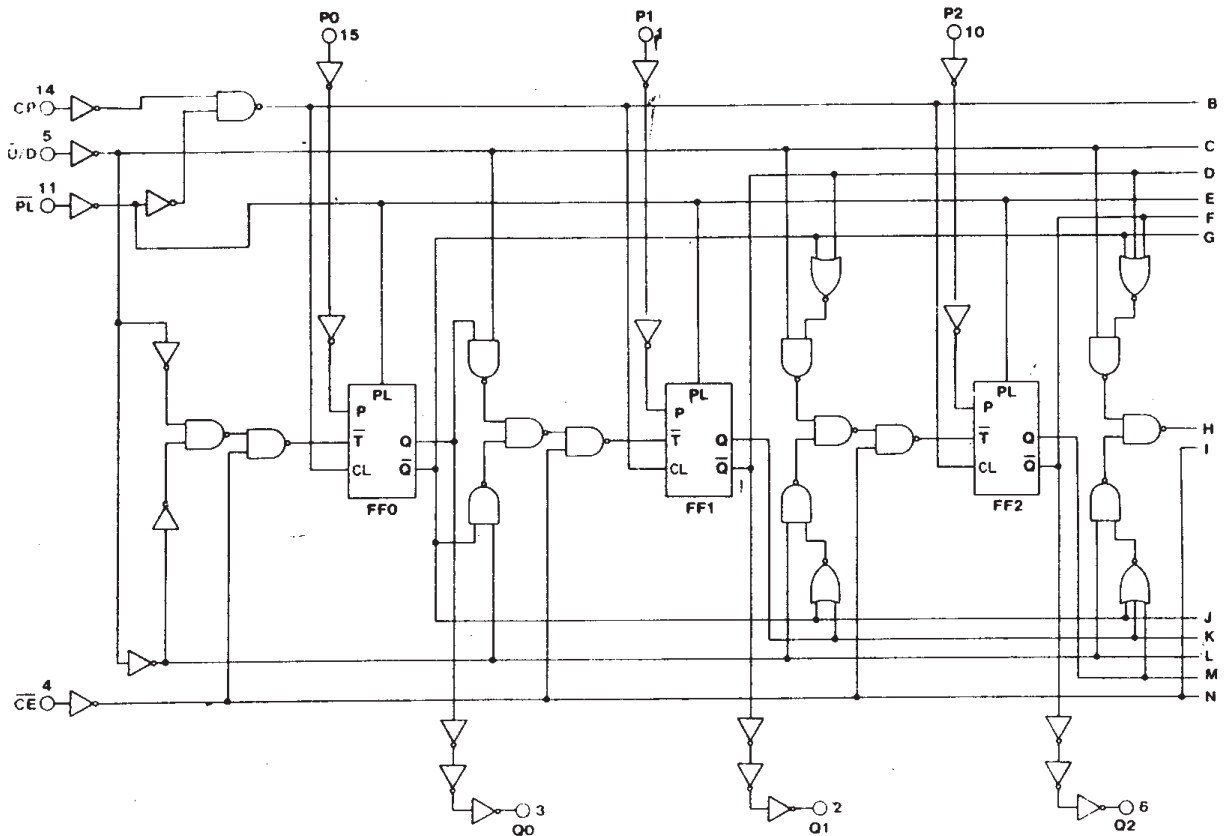


Fig. 2 - Logic diagram for HC/HCT191 (continued on next page).

92CL-38523R3

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

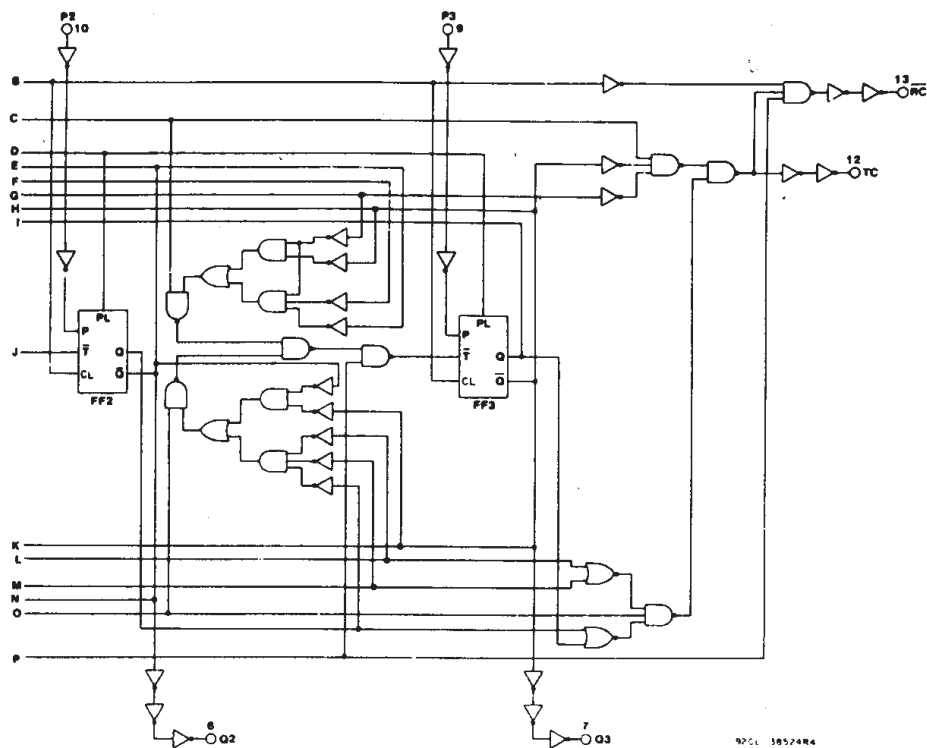


Fig. 1 - Logic diagram for HC/HCT190 (continued from previous page).

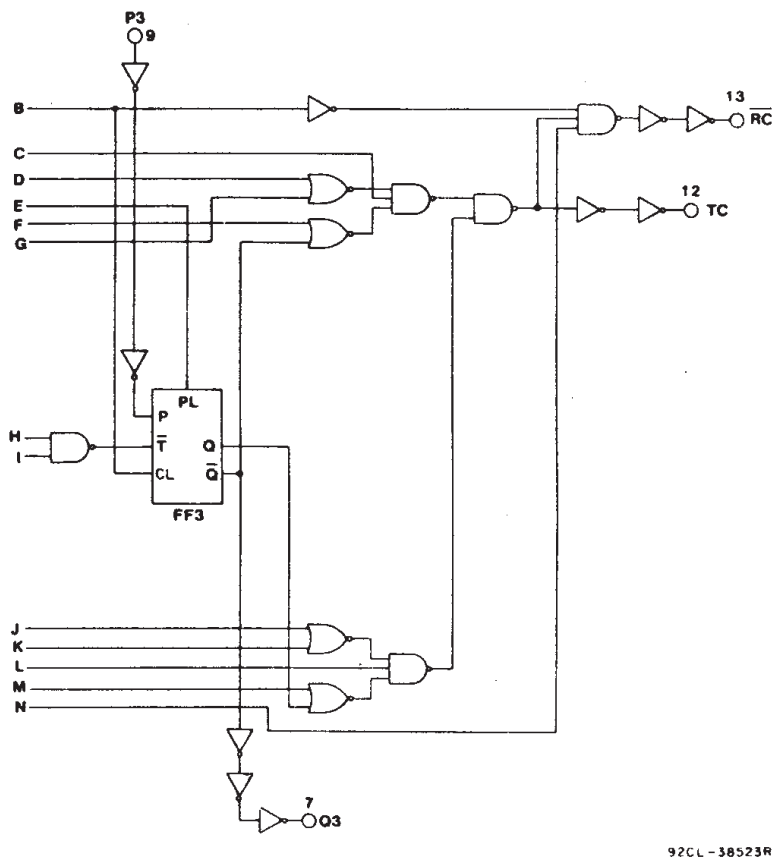


Fig. 2 - Logic diagram for HC/HCT191 (continued from previous page).

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

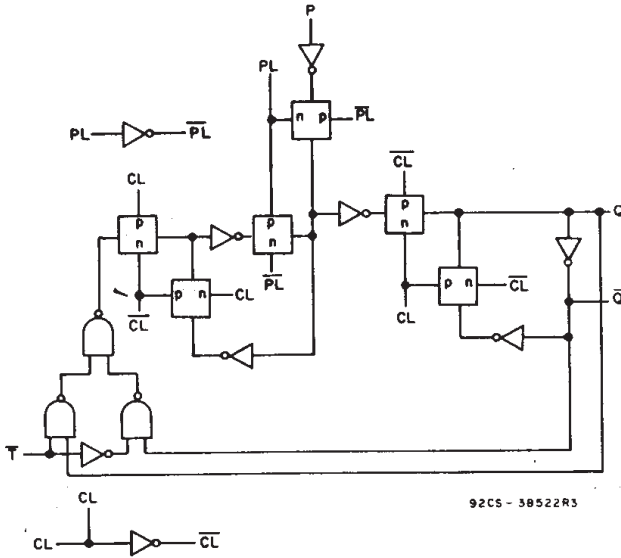


Fig. 3 - Flip-flop cell for HC/HCT190 and HC/HCT191.

TRUTH TABLE

Inputs				Function
PL	CE	U/D	CP	
H	L	L	⌄	Count Up
H	L	H	⌄	Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

Note:
 U/D or CE should be changed only when clock is high. ⌄ Low-to-high clock transition.
 X = Don't care.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	-0.5 to +7 V
(Voltages referenced to ground)	
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{CC} + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{CC} + 0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I _O) (FOR -0.5 V < V _o < V _{CC} + 0.5 V)	±25 mA
DC V _{CC} OR GROUND CURRENT, (I _{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A =Full Package Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V _i , V _o	0	V _{CC}	V
Operating Temperature, T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t _r , t _f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC190/CD54HC190 CD74HC191/CD54HC191										CD74HCT190/CD54HCT190 CD74HCT191/CD54HCT191								UNITS	
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	—	—	—	—	—	—	—	
			6	4.2	—	—	4.2	—	4.2	—	—	5.5	—	—	—	—	—	—	—	
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	—	—	—	—	—	
			6	—	—	1.8	—	1.8	—	1.8	—	5.5	—	—	—	—	—	—	—	
High-Level Output Voltage V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
CMOS Loads			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V _{IL} or V _{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
			6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
CMOS Loads			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V _{IL} or V _{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
			5.2	6	—	—	0.26	—	0.33	—	0.4									
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI _{CC} *											V _{CC} - 2.1 to 5.5	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
P0-P3	0.4
CP	1.5
PL	1.5
U/D	1.2
CE	1.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Setup Time P _n to \overline{PL} \overline{CE} to CP $\overline{U/D}$ to CP	t _{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
		2	60	—	—	—	75	—	—	—	90	—	—	—	
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
		2	90	—	—	—	115	—	—	—	135	—	—	—	
		4.5	18	—	18	—	23	—	23	—	27	—	27	—	
		6	15	—	—	—	20	—	—	—	23	—	—	—	
Hold Time P _n to \overline{PL} \overline{CE} to CP $\overline{U/D}$ to CP	t _h	2	2	—	—	—	2	—	—	—	2	—	—	—	ns
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	
		2	2	—	—	—	2	—	—	—	2	—	—	—	
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	
		2	0	—	—	—	0	—	—	—	0	—	—	—	
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Maximum Frequency*	f _{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Recovery Time	t _{REC}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
CP Pulse Width	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
\overline{PL} Pulse Width	t _w	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	

*Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable (\overline{CE})-to-clock set-up times, and count enable (\overline{CE})-to-clock hold times determine max. clock frequency. For example, with these HC devices:

$$f_{\max}(\text{CP}) = \frac{1}{\text{CP-to-TC prop. delay} + \overline{\text{CE-to-CP setup}} + \overline{\text{CE-to-CP Hold}}} = \frac{1}{42 + 12 + 2} \approx 18 \text{ MHz}$$

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	TYPICAL VALUES				UNITS
		HC		HCT		
		190	191	190	191	
Propagation Delay ($C_L = 15\text{ pF}$)						
\overline{PL} to Q_n	t_{PLH} t_{PHL}	16	16	17	17	ns
P_n to Q_n		14	14	16	16	
CP to Q_n		14	14	14	14	
CP to \overline{RC}		10	10	11	11	
CP to TC		18	18	18	18	
$\overline{U/D}$ to \overline{RC}		12	12	12	12	
$\overline{U/D}$ to TC		13	13	16	16	
\overline{CE} to \overline{RC}		10	10	11	11	
Power Dissipation Capacitance	C_{PD}^*	59	55	78	68	pF

* C_{PD} is used to determine the power consumption, per package.

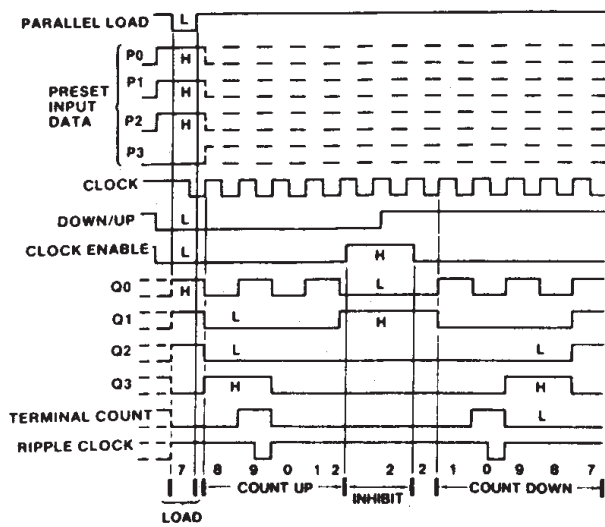
$PD = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i =input frequency f_o =output frequency C_L =output load capacitance V_{CC} =supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay \overline{PL} to Q_n	t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	ns
	t_{PHL}	4.5	—	39	—	40	—	49	—	50	—	59	—	60	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
P_n to Q_n	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
CP to Q_n	t_{PLH}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
	t_{PHL}	4.5	—	34	—	35	—	43	—	44	—	51	—	53	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
CP to \overline{RC}	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
	t_{PHL}	4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
CP to TC	t_{PLH}	2	—	210	—	—	—	265	—	—	—	315	—	—	ns
	t_{PHL}	4.5	—	42	—	42	—	53	—	53	—	63	—	63	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
$\overline{U/D}$ to \overline{RC}	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PHL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
$\overline{U/D}$ to TC	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	ns
	t_{PHL}	4.5	—	33	—	38	—	41	—	48	—	50	—	57	
		6	—	28	—	—	—	35	—	—	—	43	—	—	
\overline{CE} to \overline{RC}	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
	t_{PHL}	4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition Time Q_n, TC, \overline{RC}	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_i	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

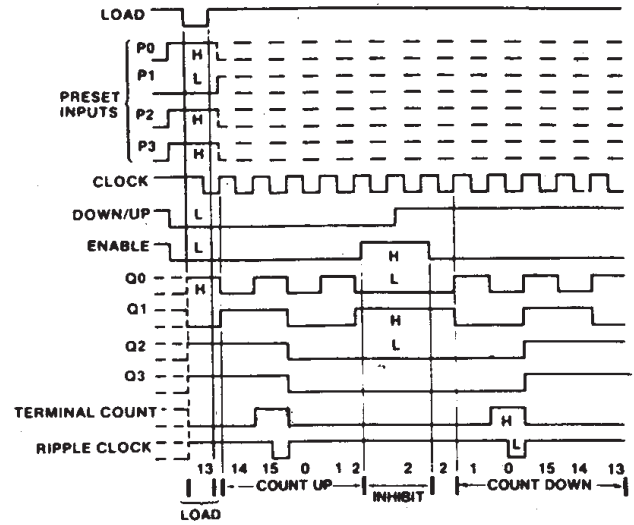
CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191

TIMING DIAGRAMS



Sequence:
 (1) Load (preset) to BCD seven (3) Inhibit
 (2) Count up to eight, nine, zero, one and two (4) Count down to one, zero, nine, eight, and seven

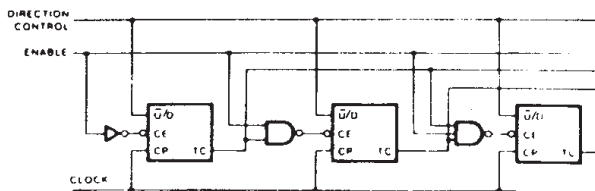
Fig. 4 - HC/HCT190 decade counters typical load, count, and inhibit sequences.



Sequence:
 (1) Load (preset) to binary thirteen (3) Inhibit
 (2) Count up to fourteen, fifteen, zero, one, and two (4) Count down to one, zero, fifteen, fourteen, and thirteen

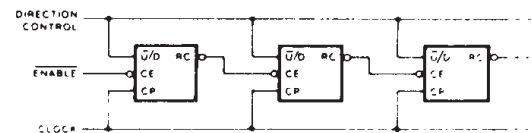
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Fig. 5 - HC/HCT191 binary counters typical load, count, and inhibit sequences.



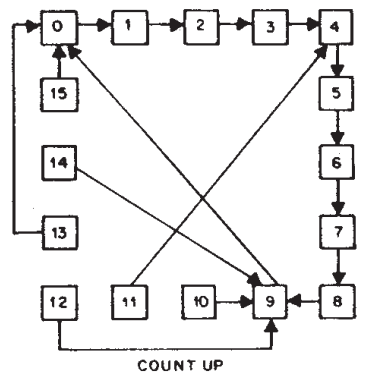
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Fig. 6 - Synchronous n-stage counter with parallel gated Terminal Count.

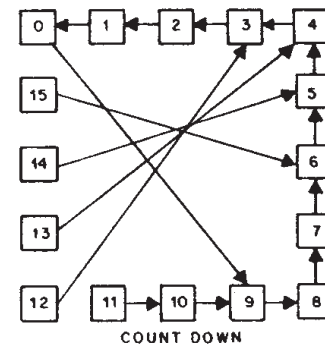


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Fig. 7 - Synchronous n-stage counter using ripple clock.



NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE OR TWO COUNTS.

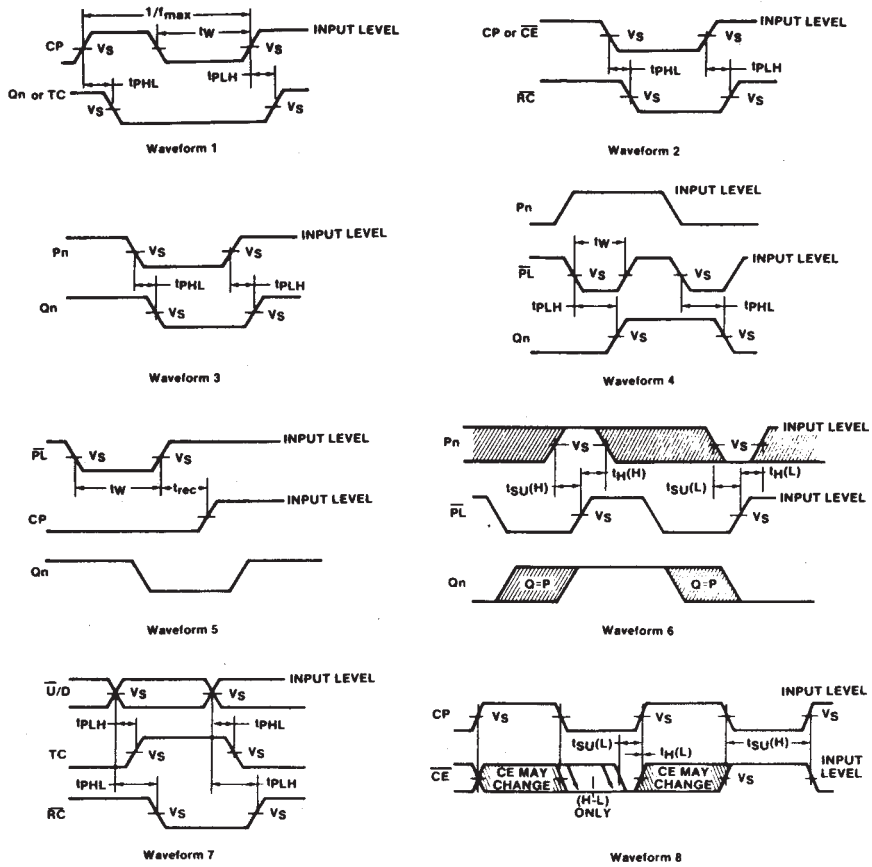


NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE OR TWO COUNTS.

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Fig. 8 - HC/HCT190 State Diagrams.

CD54/74HC190, CD54/74HCT190 CD54/74HC191, CD54/74HCT191



The shaded areas indicate when the input is permitted to change for predictable output performance

92 CL -36 403R3

	54/74HC	54/74HCT
Input Level	V _{CC}	3 V
Switching Voltage, V_S	50% V _{CC}	1.3 V

Fig. 9 - Transition, propagation delay, setup and hold, and recovery times.