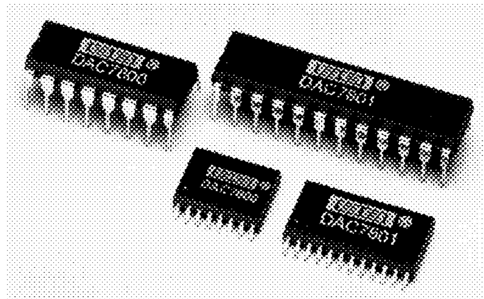
BURR - BROWN®



DAC7800
DAC7801
DAC7802

Dual Monolithic CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- TWO D/As IN A 0.3" WIDE PACKAGE
- SINGLE +5V SUPPLY
- HIGH SPEED DIGITAL INTERFACE:
  Serial—DAC7800
  8 + 4-Bit Parallel—DAC7801
  12-Bit Parallel—DAC7802
- MONOTONIC OVER TEMPERATURE
- LOW CROSSTALK: –94dB min
- FULLY SPECIFIED OVER –40°C TO +85°C

APPLICATIONS

- PROCESS CONTROL OUTPUTS
- ATE PIN ELECTRONICS LEVEL SETTING
- PROGRAMMABLE FILTERS
- PROGRAMMABLE GAIN CIRCUITS
- AUTO-CALIBRATION CIRCUITS

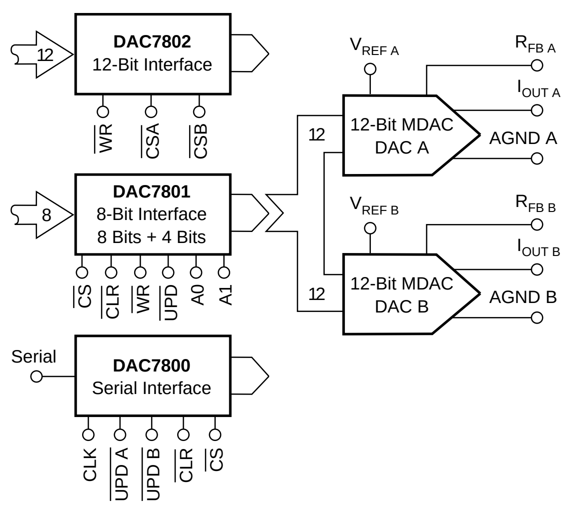
DESCRIPTION

The DAC7800, DAC7801 and DAC7802 are members of a new family of monolithic dual 12-bit CMOS multiplying digital-to-analog converters. The digital interface speed and the AC multiplying performance are achieved by using an advanced CMOS process optimized for data conversion circuits. High stability on-chip resistors provide true 12-bit integral and differential linearity over the wide industrial temperature range of –40°C to +85°C.

DAC7800 features a serial interface capable of clocking-in data at a rate of at least 10MHz. Serial data is clocked (edge triggered) MSB first into a 24-bit shift register and then latched into each D/A separately or simultaneously as required by the application. An asynchronous CLEAR control is provided for power-on reset or system calibration functions. It is packaged in a 16-pin 0.3" wide plastic DIP.

DAC7801 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each D/A. Then both D/As are updated simultaneously. DAC7801 features an asynchronous CLEAR control. DAC7801 is packaged in a 24-pin 0.3" wide plastic DIP.

DAC7802 has a single-buffered 12-bit data word interface. Parallel data is loaded (edge triggered) into the single D/A register for each D/A. DAC7802 is packaged in a 24-pin 0.3" wide plastic DIP.



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PDS-1079E
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SPECIFICATIONS

ELECTRICAL

At V_{DD} = +5VDC, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, T_A = –40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7800/7801/7802K MIN	DAC7800/7801/7802K TYP	DAC7800/7801/7802K MAX	DAC7800/7801/7802L MIN	DAC7800/7801/7802L TYP	DAC7800/7801/7802L MAX	UNITS
ACCURACY								
Resolution		12			*			Bits
Relative Accuracy				±1			±1/2	LSB
Differential Nonlinearity				±1			*	LSB
Gain Error	Measured Using $R_{FB\ A}$ and $R_{FB\ B}$. All Registers Loaded with All 1s.			±3			±1	LSB
Gain Temperature Coefficient(1)			2	5		*	*	ppm/°C
Output Leakage Current	T_A = +25°C		0.005	10		*	*	nA
	T_A = –40°C to +85°C		3	150		*	*	nA
REFERENCE INPUT								
Input Resistance		6	10	14	*	*	*	kΩ
Input Resistance Match			0.5	3		*	2	%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)		2			*			V
V_{IL} (Input Low Voltage)				0.8			*	V
I_{IN} (Input Current)	T_A = +25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8	10		*	*	pF
POWER SUPPLY								
V_{DD}		4.5		5.5	*		*	V
I_{DD}			0.2	2		*	*	mA
Power Supply Rejection	V_{DD} from 4.5V to 5.5V			0.002			*	%/%

* Same specification as for DAC7800/7801/7802K.

AC PERFORMANCE

OUTPUT OP AMP IS OPA602.

At V_{DD} = +5VDC, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, T_A = +25°C unless otherwise noted. These specifications are fully characterized but not subject to test.

PARAMETER	CONDITIONS	DAC7800/7801/7802K MIN	DAC7800/7801/7802K TYP	DAC7800/7801/7802K MAX	DAC7800/7801/7802L MIN	DAC7800/7801/7802L TYP	DAC7800/7801/7802L MAX	UNITS
OUTPUT CURRENT SETTLING TIME	To 0.01% of Full Scale R_L = 100Ω, C_L = 13pF		0.4	0.8		*	*	µs
DIGITAL-TO-ANALOG GLITCH IMPULSE	$V_{REF\ A}$ = $V_{REF\ B}$ = 0V R_L = 100Ω, C_L = 13pF		0.9			*		nV-s
AC FEEDTHROUGH	f_{VREF} = 10kHz		–75	–72		*	*	dB
OUTPUT CAPACITANCE	DAC Loaded with All 0s		30	50		*	*	pF
	DAC Loaded with All 1s		70	100		*	*	pF
CHANNEL-TO-CHANNEL ISOLATION								
$V_{REF\ A}$ to $I_{OUT\ B}$	$f_{VREF\ A}$ = 10kHz $V_{REF\ B}$ = 0V, Both DACs Loaded with 1s	–90	–94		*	*		dB
$V_{REF\ B}$ to $I_{OUT\ A}$	$f_{VREF\ B}$ = 10kHz $V_{REF\ A}$ = 0V, Both DACs Loaded with 1s	–90	–101		*	*		dB
DIGITAL CROSSTALK	Full Scale Transition R_L = 100Ω, C_L = 13pF		0.9			*		nV-s

NOTE: (1) Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

At T_A = +25°C unless otherwise noted.

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	–0.3, V_{DD}
Digital Input to DGND	–0.3, V_{DD} + 0.3
$V_{REF\ A}$, $V_{REF\ B}$ to AGND	±25V
$V_{REF\ A}$, $V_{REF\ B}$ to DGND	±25V
$I_{OUT\ A}$, $I_{OUT\ B}$ to AGND	–0.3, V_{DD}
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC7800KP	16-Pin PDIP	180
DAC7800LP	16-Pin PDIP	180
DAC7800KU	16-Pin SOIC	211
DAC7800LU	16-Pin SOIC	211
DAC7801KP	24-Pin DIP	243
DAC7801LP	24-Pin DIP	243
DAC7801KU	24-Pin SOIC	239
DAC7801LU	24-Pin SOIC	239
DAC7802KP	24-Pin DIP	243
DAC7802LP	24-Pin DIP	243
DAC7802KU	24-Pin SOIC	239
DAC7802LU	24-Pin SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure.

Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

Digital Inputs: All digital inputs of the DAC780X family incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

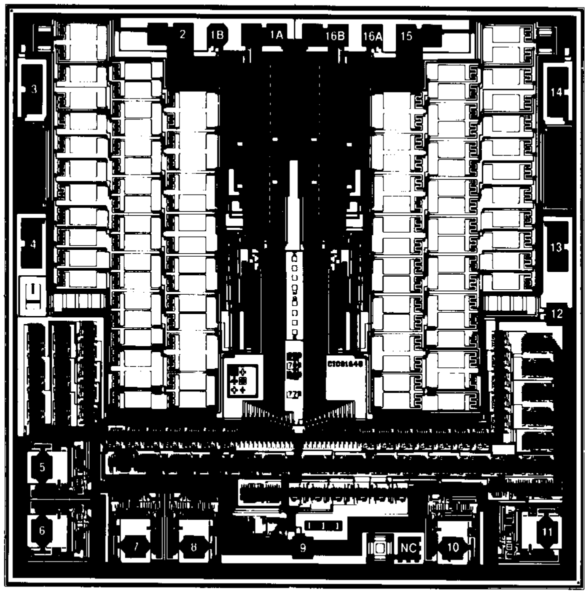
Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. AGND, I_{OUT}, and R_{FB} show some sensitivity. Failure to observe ESD handling procedures could result in catastrophic device failure.

ORDERING INFORMATION

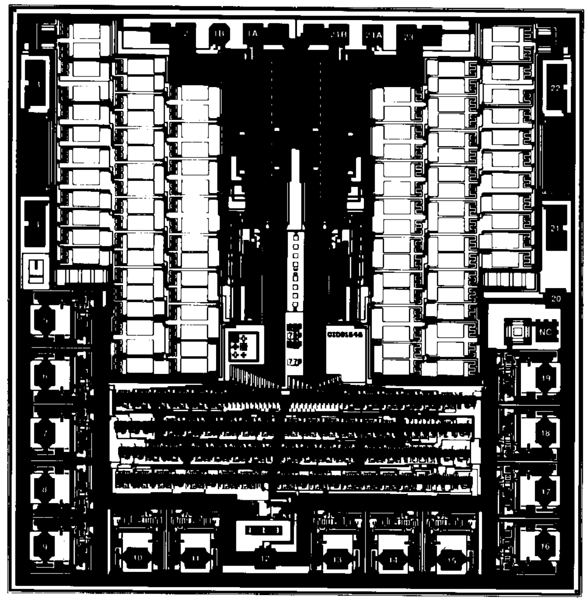
MODEL	RELATIVE ACCURACY	GAIN ERROR	PACKAGE
DAC7800KP	±1LSB	±3LSB	16-Pin DIP
DAC7800KU(1)			16-Lead SO
DAC7800LP	±1/2LSB	±1LSB	16-Pin DIP
DAC7800LU			16-Lead SO
DAC7801KP	±1LSB	±3LSB	24-Pin DIP
DAC7801KU			24-Lead SO
DAC7801LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7801LU			24-Lead SO
DAC7802KP	±1LSB	±3LSB	24-Pin DIP
DAC7802KU(1)			24-Lead SO
DAC7802LP	±1/2LSB	±1LSB	24-Pin DIP
DAC7802LU			24-Lead SO

NOTE: (1) Available with Tape and Reel. Add "-TR" to basic model number.

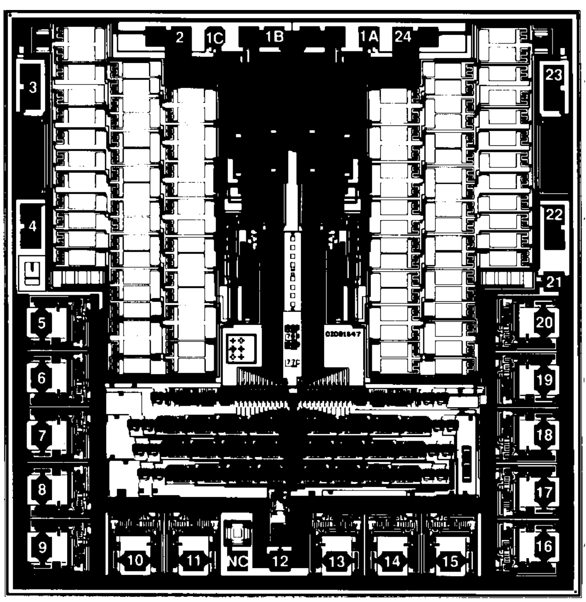
DICE INFORMATION



DAC7800 DIE TOPOGRAPHY



DAC7801 DIE TOPOGRAPHY



DAC7802 DIE TOPOGRAPHY

MECHANICAL INFORMATION

DAC7800	MILS (0.001")	MILLIMETERS
Die Size	131 x 136 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

Substrate Bias: $+V_{DD}$

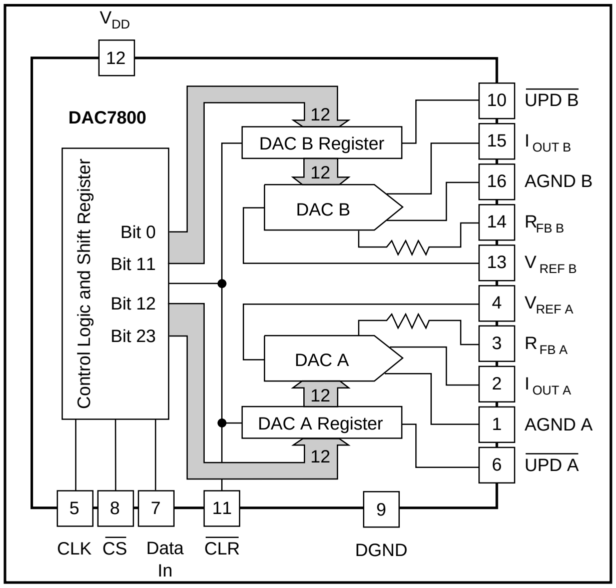
DAC7801	MILS (0.001")	MILLIMETERS
Die Size	131 x 134 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metallization		Aluminum

Substrate Bias: $+V_{DD}$

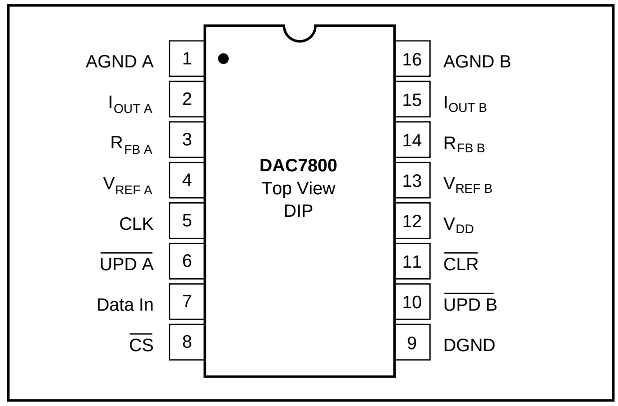
DAC7802	MILS (0.001")	MILLIMETERS
Die Size	131 x 121 ±5	3.33 x 3.07 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

Substrate Bias: $+V_{DD}$

BLOCK DIAGRAM



PIN CONFIGURATION

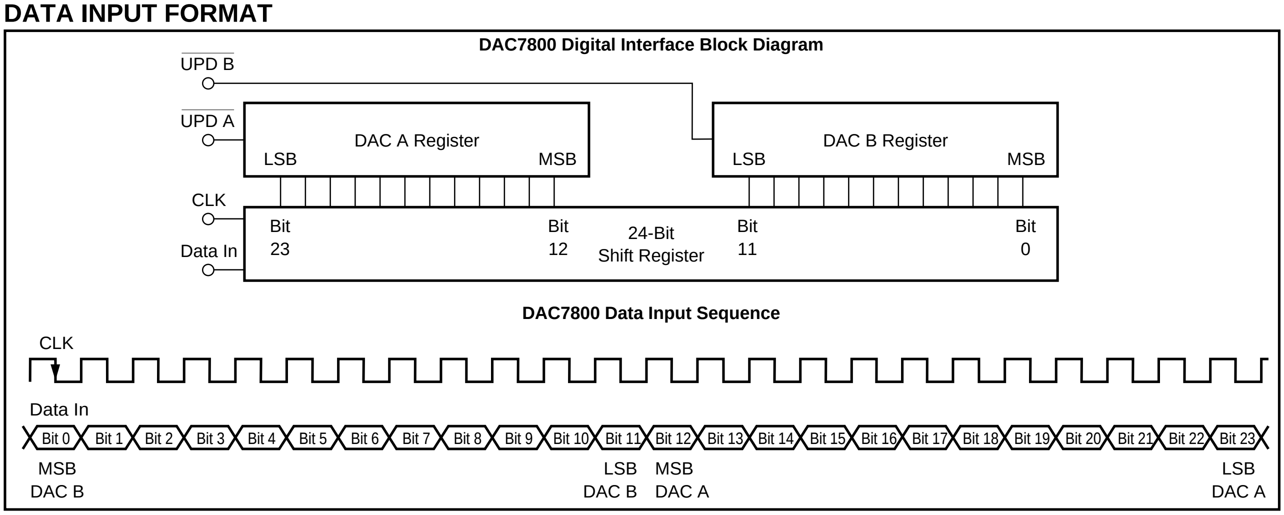


LOGIC TRUTH TABLE

CLK	$\overline{\text{UPD A}}$	$\overline{\text{UPD B}}$	$\overline{\text{CS}}$	$\overline{\text{CLR}}$	FUNCTION
X	X	X	X	0	All register contents set to 0's (asynchronous).
X	X	X	1	X	No data transfer.
↓	X	X	0	1	Input data is clocked into input register (location Bit 23) and previous data shifts.
X	0	1	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A.
X	1	0	0	1	Input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.
X	0	0	0	1	Input register bits 23 (LSB)—12 (MSB) are loaded into DAC A, and input register bits 11 (LSB)—0 (MSB) are loaded into DAC B.

X = Don't care. ↓ means falling edge triggered.

DATA INPUT FORMAT

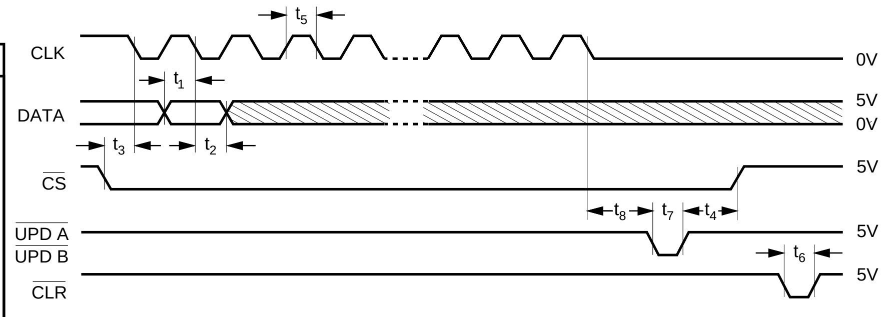


DAC7800 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, T_A = –40°C to +85°C.

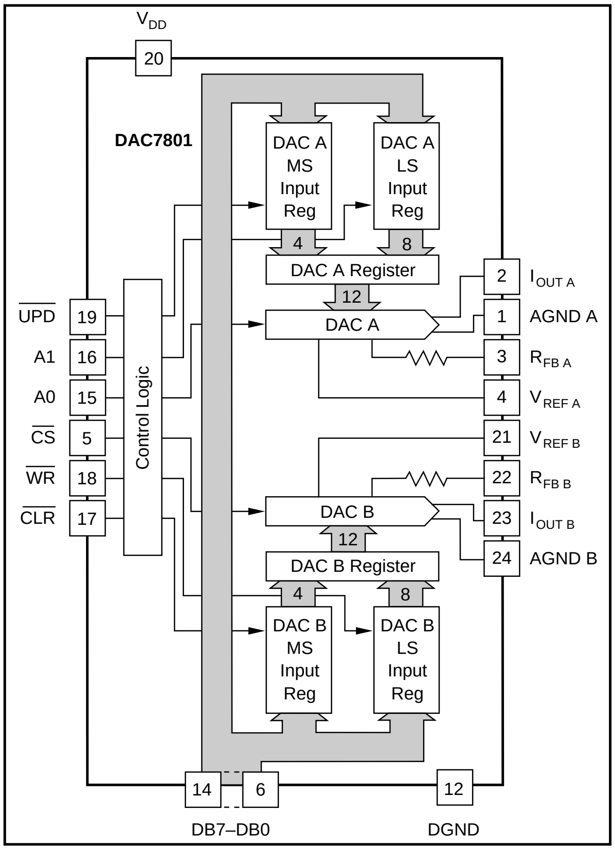
PARAMETER	MINIMUM
t_1 — Data Setup Time	15ns
t_2 — Data Hold Time	15ns
t_3 — Chip Select to CLK, Update, Data Setup Time	15ns
t_4 — Chip Select to CLK, Update, Data Hold Time	40ns
t_5 — CLK Pulse Width	40ns
t_6 — Clear Pulse Width	40ns
t_7 — Update Pulse Width	40ns
t_8 — CLK Edge to $\overline{UPD\ A}$ or $\overline{UPD\ B}$	15ns



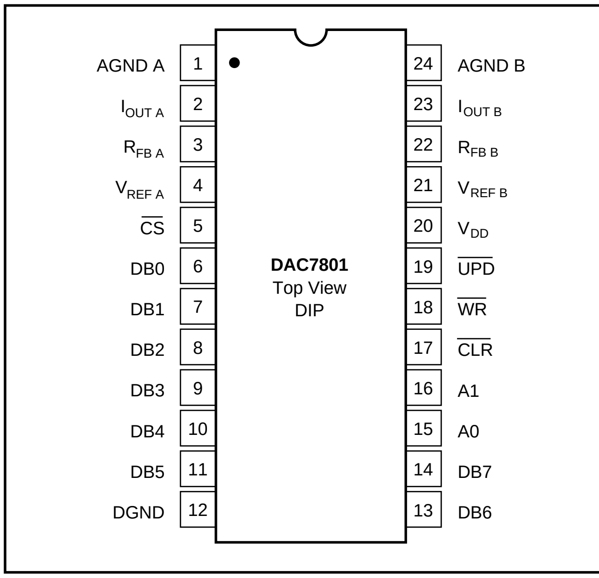
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7801

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)–DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7–DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)–DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

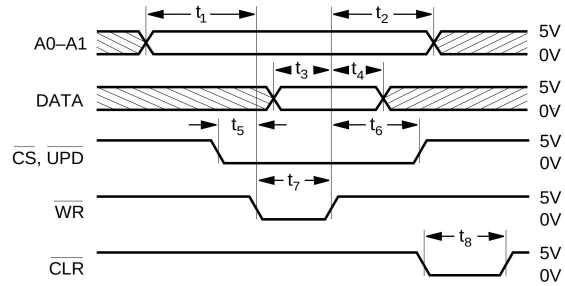
X = Don't care.

DAC7801 (CONT)

TIMING CHARACTERISTICS

V_{DD} = +5V, $V_{REF\ A}$ = $V_{REF\ B}$ = +10V, T_A = –40°C to +85°C.

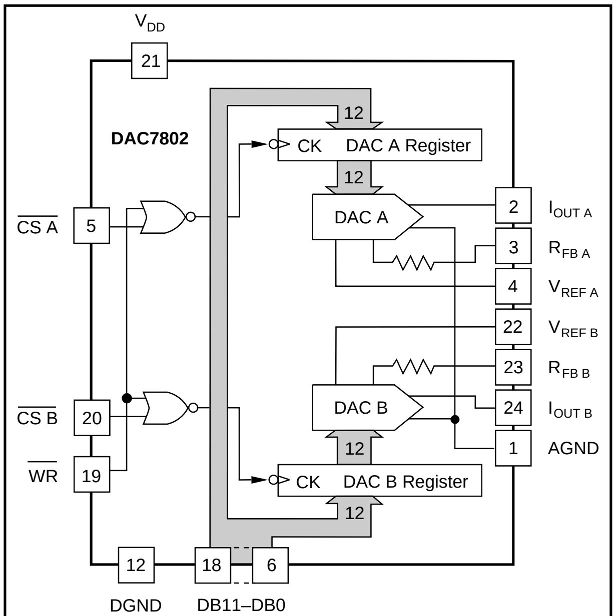
PARAMETER	MINIMUM
t_1 — Address Valid to Write Setup Time	10ns
t_2 — Address Valid to Write Hold Time	10ns
t_3 — Data Setup Time	30ns
t_4 — Data Hold Time	10ns
t_5 — Chip Select or Update to Write Setup Time	0ns
t_6 — Chip Select or Update to Write Hold Time	0ns
t_7 — Write Pulse Width	40ns
t_8 — Clear Pulse Width	40ns



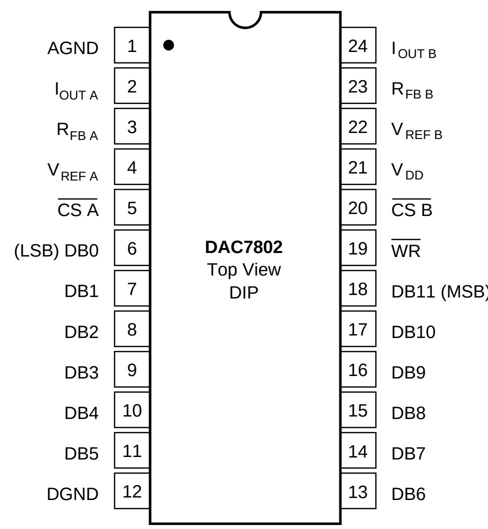
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

DAC7802

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC TRUTH TABLE

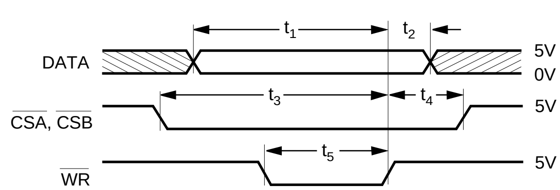
$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↑	↑	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC
0	1	↑	DAC A Register Loaded from Data Bus
1	0	↑	DAC B Register Loaded from Data Bus
0	0	↑	DAC A and DAC B Registers Loaded from Data Bus

X = Don't care. ↑ means rising edge triggered.

TIMING CHARACTERISTICS

At V_{DD} = +5V, and T_A = –40ºC to +85ºC.

PARAMETER	MINIMUM
t_1 - Data Setup Time	20ns
t_2 - Data Hold Time	15ns
t_3 - Chip Select to Write Setup Time	30ns
t_4 - Chip Select to Write Hold Time	0ns
t_5 - Write Pulse Width	30ns

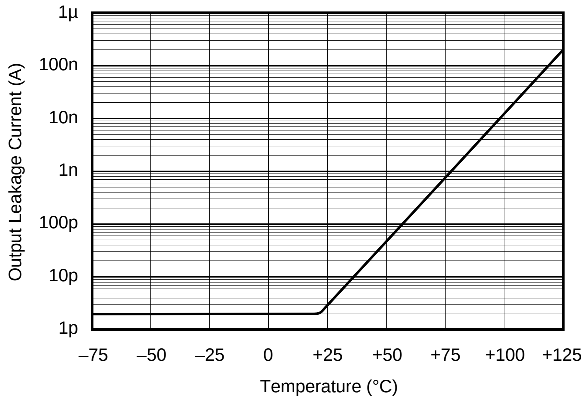


NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns. (2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

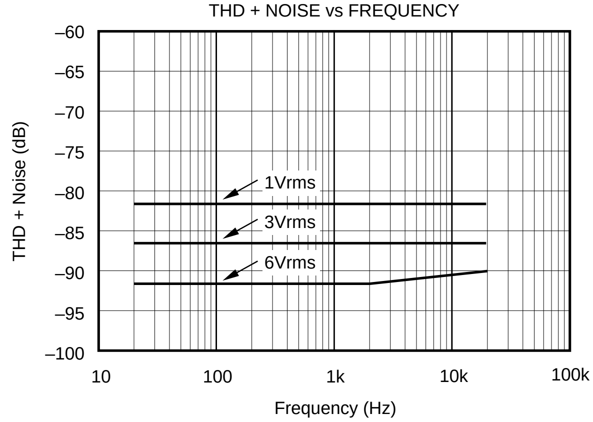
TYPICAL PERFORMANCE CURVES

OUTPUT OP AMP IS OPA602.
$T_A = +25°C$, $V_{DD} = +5V$.

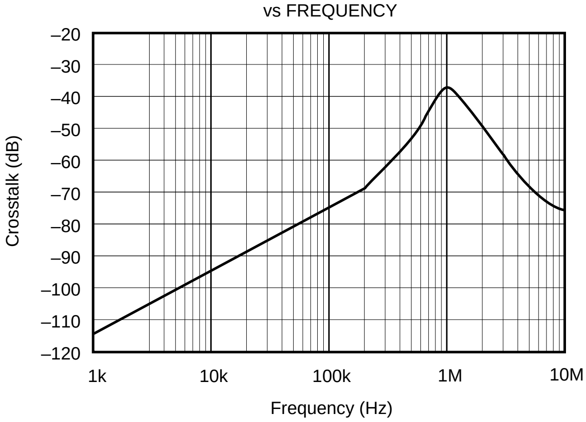
OUTPUT LEAKAGE CURRENT
vs TEMPERATURE



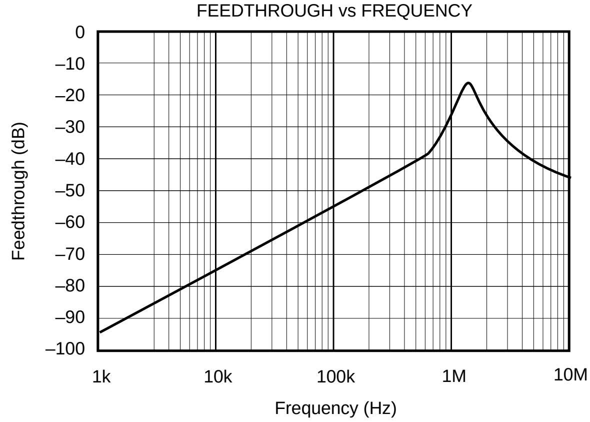
THD + NOISE vs FREQUENCY



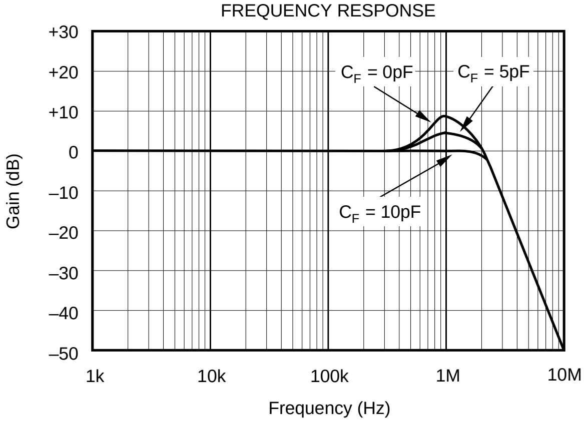
CHANNEL-TO-CHANNEL ISOLATION
vs FREQUENCY



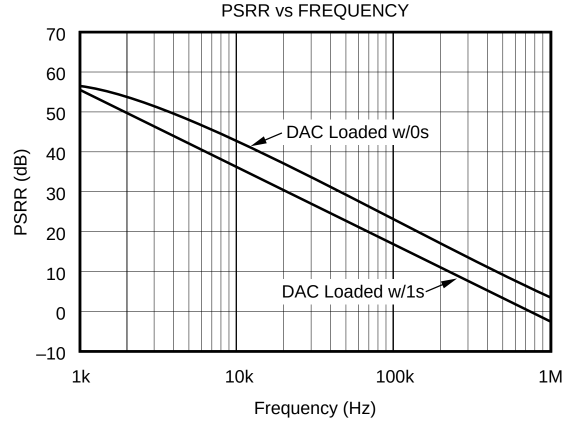
FEEDTHROUGH vs FREQUENCY



FREQUENCY RESPONSE



PSRR vs FREQUENCY



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC780X is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figures 5 and 7.

OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT\ A}$ and $I_{OUT\ B}$ with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT\ A}$ or $I_{OUT\ B}$ to AGND.

CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

MULTIPLYING FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.01% of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC780X. The current from the $V_{REF\ A}$ pin is switched between $I_{OUT\ A}$ and AGND by 12 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.

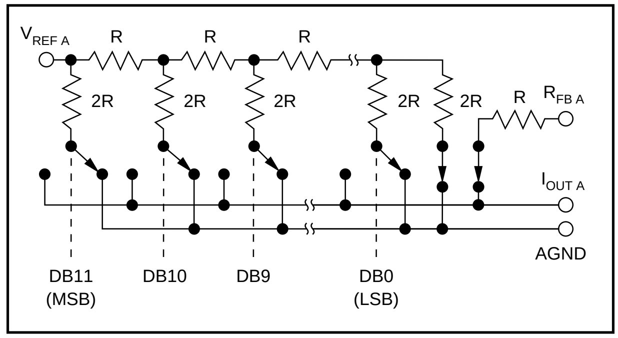


FIGURE 1. Simplified Circuit Diagram for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB\ A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every 10°C. R_O is the equivalent output resistance of the D/A and it varies with input code.

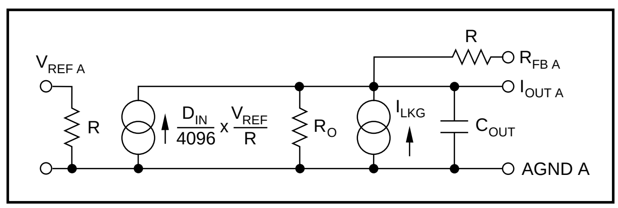


FIGURE 2. Equivalent Circuit for DAC A.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC780X incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC780X are designed to operate on V_{DD} = +5V ±10%. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1µF tantalum recommended) should be located close to the D/A. AGND and

DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pins of the DAC780X as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC780X directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC780X should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where R_O = infinity), the R_O will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of R_O is nonlinear with code, and the largest steps in R_O occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good nonlinearity the op amp offset should be much less than 1/2LSB.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC780X in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

BIPOLAR CONFIGURATION

Figure 5 shows the DAC780X in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table III.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE II. Unipolar Output Code.

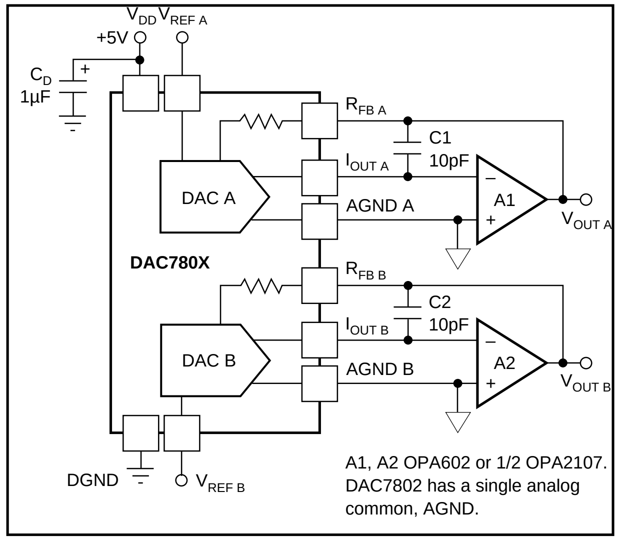


FIGURE 3. Unipolar Configuration.

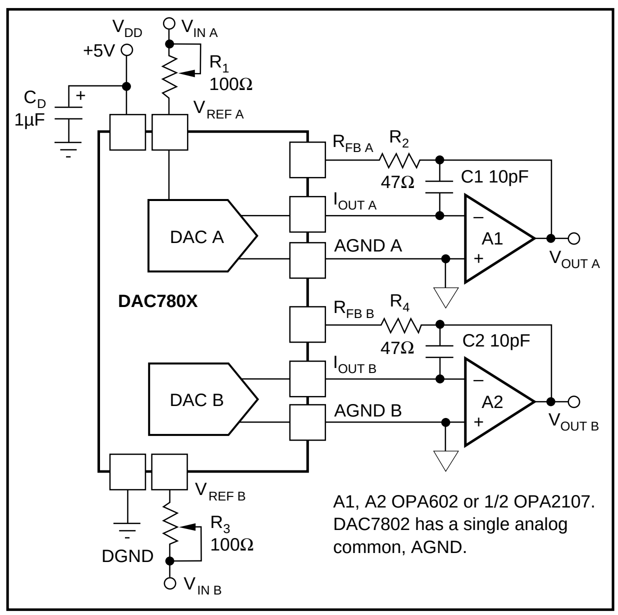


FIGURE 4. Unipolar Configuration with Gain Trim.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R5–R7 and R8–R10 should be ratio-matched to 0.01% to ensure the specified gain error performance.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 6 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE III. Bipolar Output Code.

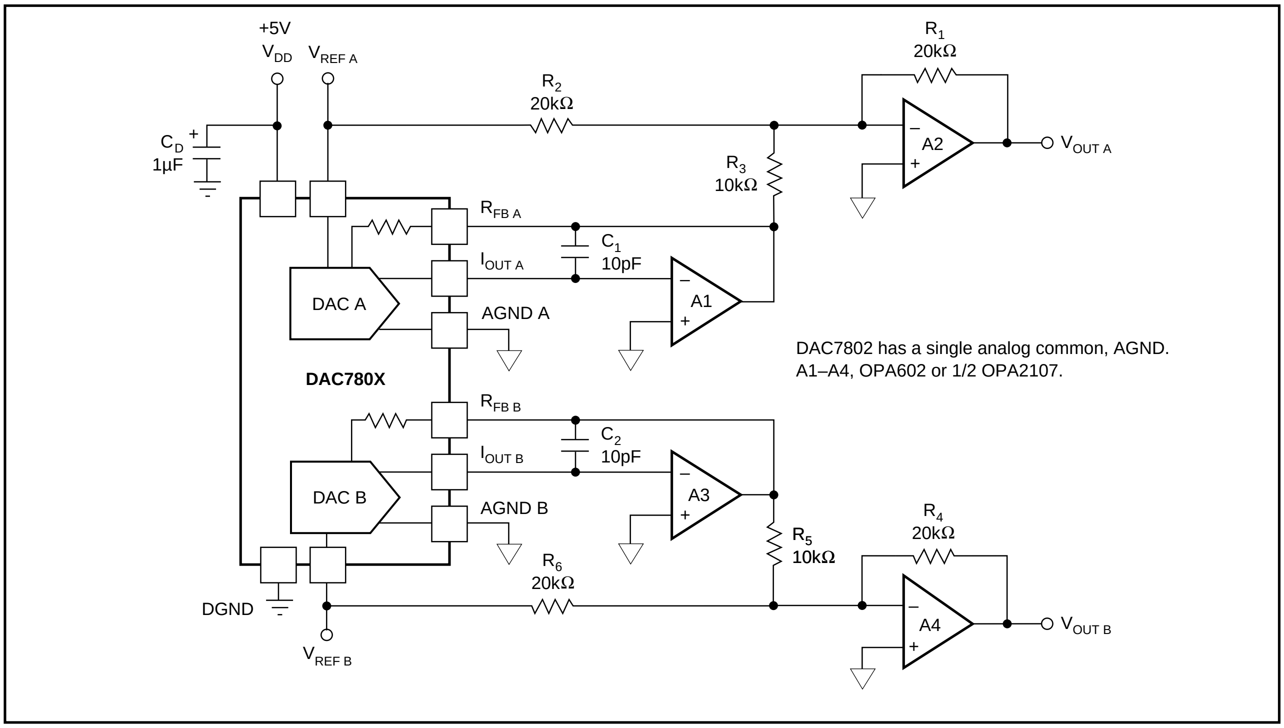


FIGURE 5. Bipolar Configuration.

APPLICATIONS

12-BIT PLUS SIGN DACS

For a bipolar DAC with 13 bits of resolution, two solutions are possible. As shown in Figure 7, the addition of a precision difference amplifier and a high speed JFET switch provides a 12-bit plus sign voltage-output DAC. When the switch selects the op amp output, the difference amplifier serves as a non-inverting output buffer. If the analog ground side of the switch is selected, the output of the difference amplifier is inverted.

Another option, shown in Figure 8, also produces a 12-bit plus sign output without the additional switch and digital control line.

DIGITALLY PROGRAMMABLE ACTIVE FILTER

DAC780X are shown in Figure 9 in a digitally programmable active filter application. The design is based on the state-variable filter, Burr-Brown UAF42, an active filter topology that offers stable and repeatable filter characteristics.

DAC1 and DAC2 can be updated in parallel with a single word to set the center frequency of the filter. DAC 4, which makes use of the uncommitted op amp in UAF42, sets the Q of the filter. DAC3 sets the gain of the filter transfer function without changing the Q of the filter. The reverse is also true.

The center frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance of the D/A (typical value, 10kΩ) and C the internal capacitor value (1000pF) of the UAF42. External capacitors can be added to lower the center frequency of the filter. But the highest center frequency for this circuit will be about 16kHz because the effective series resistance of the D/A cannot be less than 10kΩ.

Note that the ladder resistance of the D/A may vary from device to device. Thus, for best tracking, DAC2 and DAC3 should be in the same package. Some calibration may be necessary from one filter to another.

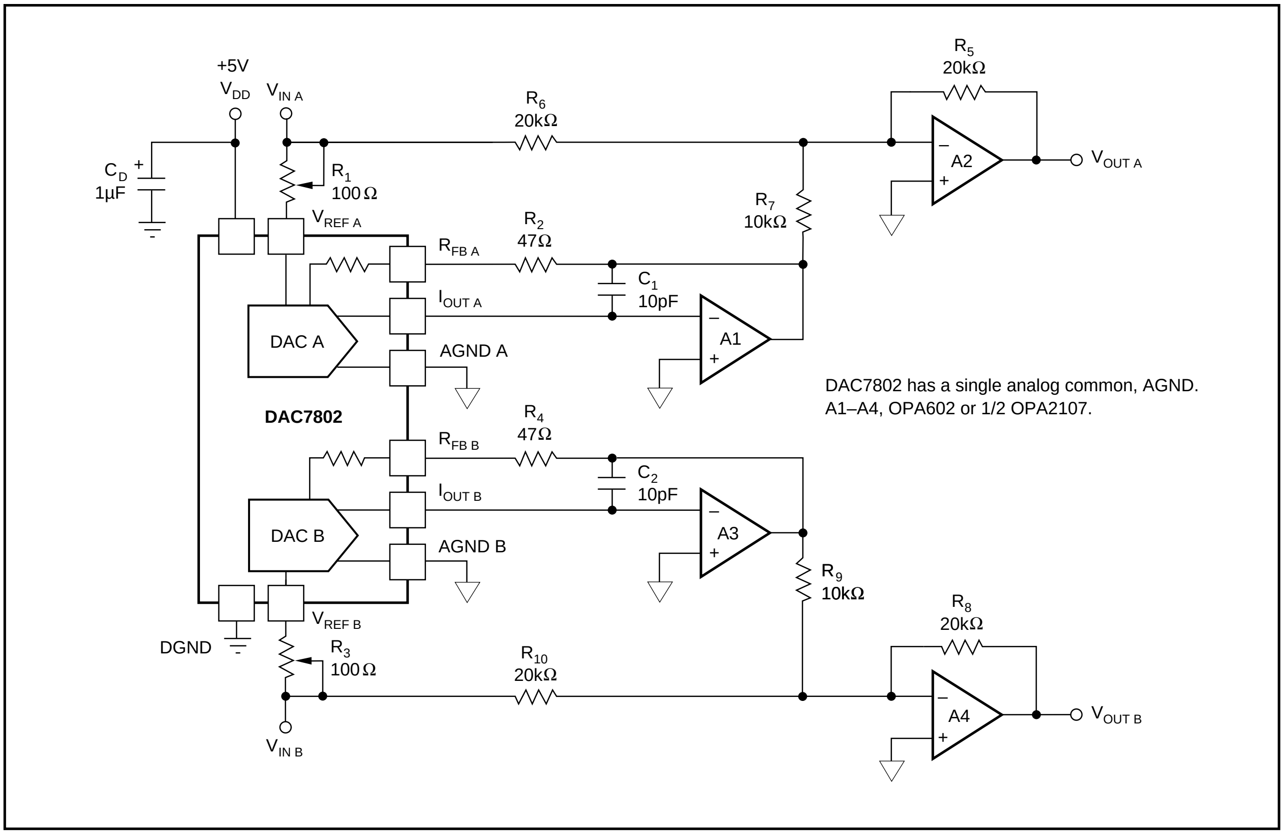


FIGURE 6. Bipolar Configuration with Gain Trim.

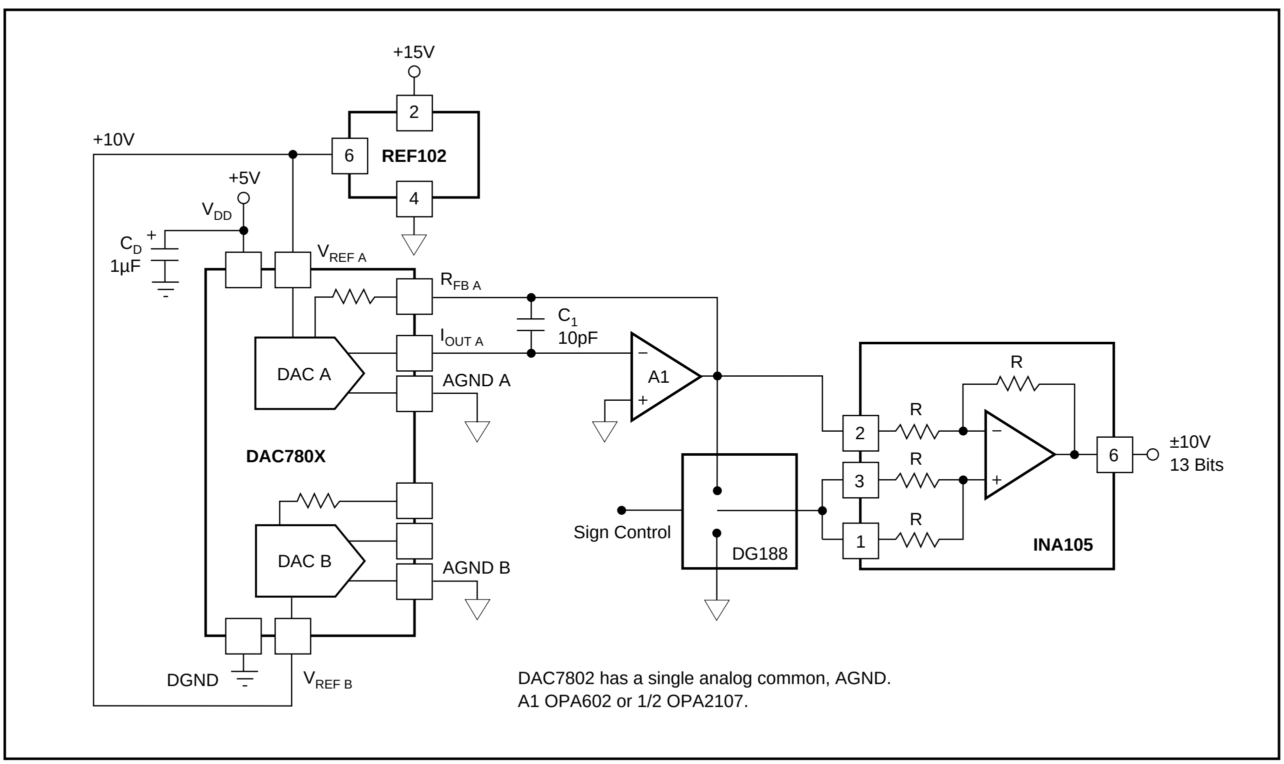


FIGURE 7. 12-Bit Plus Sign DAC.

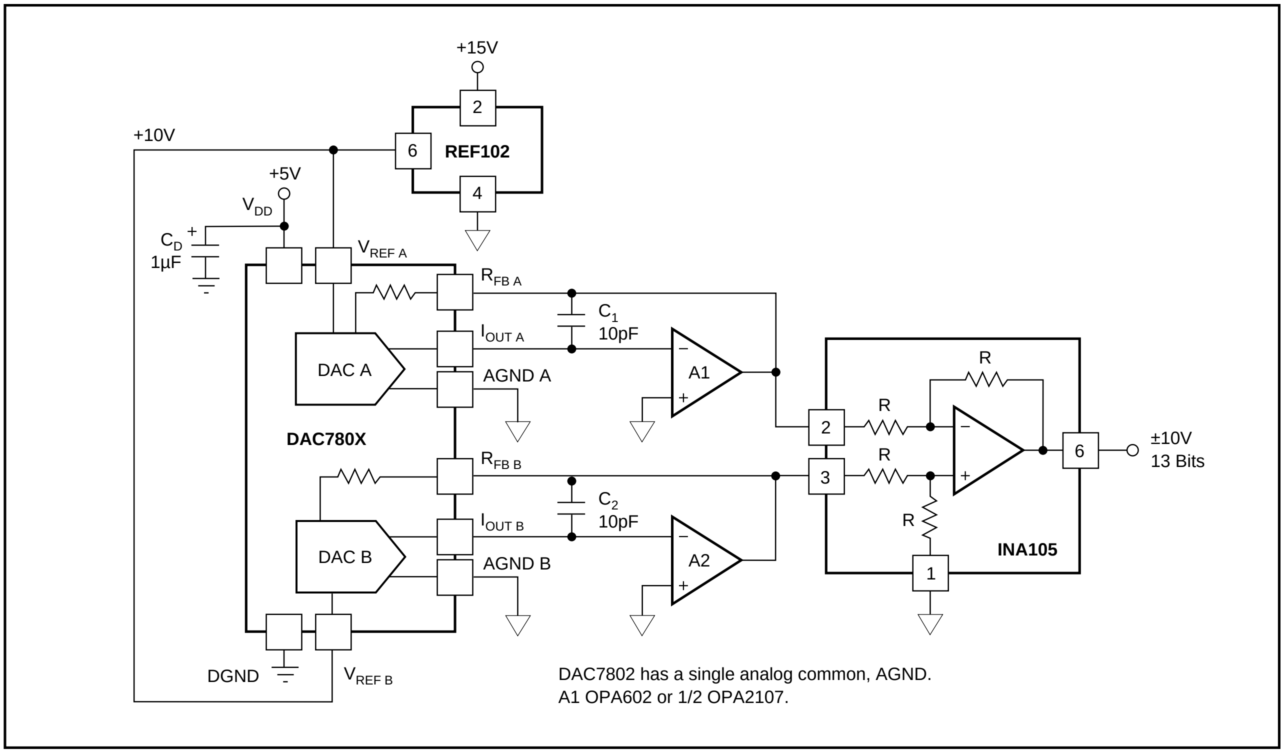


FIGURE 8. 13-Bit Bipolar DAC.

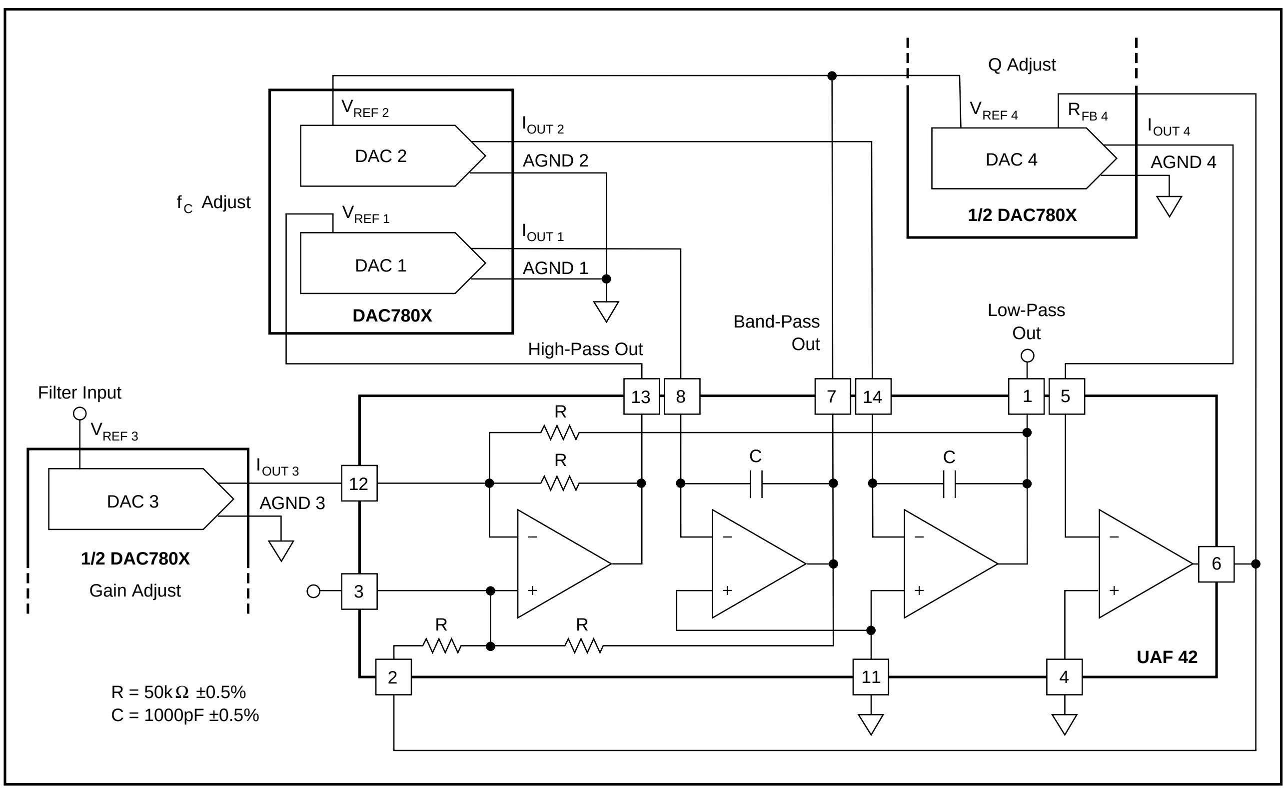


FIGURE 9. Digitally Programmable Universal Active Filter.