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INA102

Low Power
INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW QUIESCENT CURRENT: 750μA max**
- **INTERNAL GAINS: 1, 10, 100, 1000**
- **LOW GAIN DRIFT: 5ppm/°C max**
- **HIGH CMR: 90dB min**
- **LOW OFFSET VOLTAGE DRIFT:**
  2μV/°C max
- **LOW OFFSET VOLTAGE: 100μV max**
- **LOW NONLINEARITY: 0.01% max**
- **HIGH INPUT IMPEDANCE: $10^{10}\Omega$**

APPLICATIONS

- **AMPLIFICATION OF SIGNALS FROM**
  SOURCES SUCH AS:
  Strain Gages (Weigh Scale Applications)
  Thermocouples
  Bridge Transducers
- **REMOTE TRANSDUCER AMPLIFIER**
- **LOW-LEVEL SIGNAL AMPLIFIER**
- **MEDICAL INSTRUMENTATION**
- **MULTICHANNEL SYSTEMS**
- **BATTERY POWERED EQUIPMENT**

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery-powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. A gain drift of 5ppm/°C in low gains can then be achieved without external adjustment. When higher-than-specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.
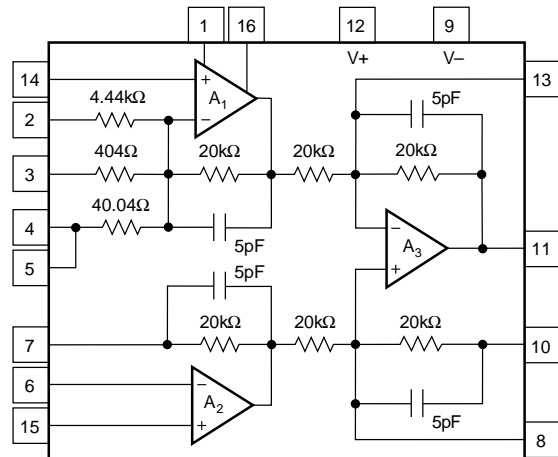
PDS-523G
Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2, unless otherwise noted.

PARAMETER	CONDITIONS	INA102AG MIN	INA102AG TYP	INA102AG MAX	INA102CG MIN	INA102CG TYP	INA102CG MAX	INA102KP/INA102AU MIN	INA102KP/INA102AU TYP	INA102KP/INA102AU MAX	UNITS
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation, External, ±20%			$G = 1 + (40k/R_G)$[1]				*			*	V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.16			0.08			0.21	%
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.19			0.11			0.44	%
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.37			0.21			0.52	%
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			*	ppm/°C
G = 10				15			10			*	ppm/°C
G = 100				20			15			*	ppm/°C
G = 1000				30			20			*	ppm/°C
Nonlinearity, DC											
G = 1	T_A = +25°C			0.03			0.01			*	% of FS
G = 10	T_A = +25°C			0.03			0.01			*	% of FS
G = 100	T_A = +25°C			0.05			0.02			*	% of FS
G = 1000	T_A = +25°C			0.1			0.05			*	% of FS
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			*	% of FS
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			*	% of FS
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.075			0.03			*	% of FS
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.15			0.1			*	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	±(|V_{CC}| − 2.5)			*			*			V
Current		±1			*			*			mA
Short Circuit Current[2]			2			*			*		mA
Output Impedance, G = 1000			0.1			*			*		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[3]	T_A = +25°C		±300 ±300/G			±100 ±200/G				*	µV
INA102AU									**±500 ±300/G**		µV
vs Temperature			±5 ±10/G			±2 ±5/G				*	µV/°C
vs Supply			±40 ±50/G			±10 ±20/G				*	µV/V
vs Time			±(20 + 30/G)			*				*	µV/mo
BIAS CURRENT											
Initial Bias Current											
(Each Input)	$T_A = T_{MIN}$ to T_{MAX}		25	50		6	30		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
vs Supply			±0.1			*			*		nA/V
Initial Offset Current	$T_A = T_{MIN}$ to T_{MAX}		±2.5	±15		±2.5	±10		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
IMPEDANCE											
Differential			10^{10} ‖ 2			*			*		Ω ‖ pF
Common-Mode			10^{10} ‖ 2			*			*		Ω ‖ pF
VOLTAGE RANGE											
Range, Linear Response	$T_A = T_{MIN}$ to T_{MAX}	±(|V_{CC}| − 4.5)			*			*			V
CMR With 1kΩ Source Imbalance											
G = 1	DC to 60Hz	80	94		90	*		75	*		dB
G = 10	DC to 60Hz	80	100		90	*		*	*		dB
G = 10 to 1000	DC to 60Hz	80	100		90	*		*	*		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			1			*			*		µVp-p
Density, G = 1000: f_O = 10Hz			30			*			*		nV/√Hz
f_O = 100Hz			25			*			*		nV/√Hz
f_O = 1kHz			25			*			*		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			*			*		pAp-p
Density: f_O = 10Hz			0.3			*			*		pA/√Hz
f_O = 100Hz			0.2			*			*		pA/√Hz
f_O = 1kHz			0.15			*			*		pA/√Hz

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA102AG MIN	INA102AG TYP	INA102AG MAX	INA102CG MIN	INA102CG TYP	INA102CG MAX	INA102KP/INA102AU MIN	INA102KP/INA102AU TYP	INA102KP/INA102AU MAX	UNITS
DYNAMIC RESPONSE											
Small Signal, ±3dB Flatness	V_{OUT} = 0.1Vrms										
G = 1			300			*			*		kHz
G = 10			30			*			*		kHz
G = 100			3			*			*		kHz
G = 1000			0.3			*			*		kHz
Small Signal, ±1% Flatness	V_{OUT} = 0.1Vrms										
G = 1			30			*			*		kHz
G = 10			3			*			*		kHz
G = 100			0.3			*			*		kHz
G = 1000			0.03			*			*		kHz
Full Power, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	1.7	2.5		*	*		*	*		kHz
Slew Rate, G = 1 to 100	V_{OUT} = 10V, R_L = 10kΩ	0.1	0.15		*	*		*	*		V/µs
Settling Time	R_L = 10kΩ, C_L = 100pF										
0.1%: G = 1	10V Step		50			*			*		µs
G = 100			360			*			*		µs
G = 1000			3300			*			*		µs
0.01%: G = 1	10V Step		60			*			*		µs
G = 100			500			*			*		µs
G = 1000			4500			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±3.5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V, T_A = T_{MIN} to T_{MAX}		±500	±750		*	*		*	*	µA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
INA102AU								**−25**		**+85**	°C
Operation	R_L > 50kΩ[2]	−25		+85	*		*	−25		+85	°C
Storage		−65		+150	*		*	−55		+125	°C

*Specification same as for INA102AG.
NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_G will add to the gain error if gains other than 1, 10, 100, or 1000 are set externally. (2) At high temperature, output drive current is limited. An external buffer can be used if required. (3) Adjustable to zero.

PIN CONFIGURATION

Top View   **DIP/SOIC**

Offset Adjust	1	16	Offset Adjust
x 10 Gain	2	15	+In
x 100 Gain	3	14	−In
x 1000 Gain	4	13	Filter
x 1000 Gain Sense	5	12	$+V_{CC}$
Gain Sense	6	11	Output
Gain Set	7	10	Common
CMR Trim	8	9	$-V_{CC}$
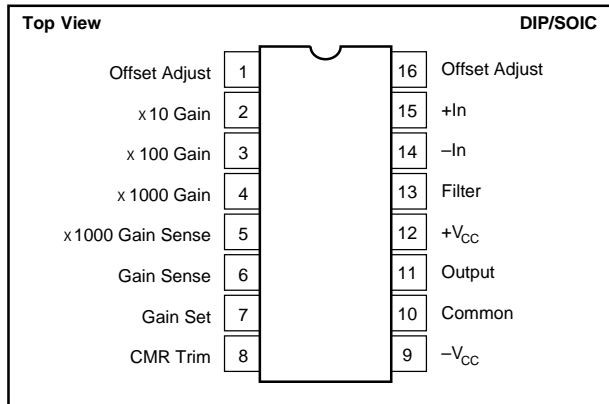
ABSOLUTE MAXIMUM RATINGS

Supply .... ±18V
Input Voltage Range .... ±V_{CC}
Operating Temperature Range .... −25°C to +85°C
Storage Temperature Range: Ceramic .... −65°C to +150°C
                                                Plastic, SOIC .... −55°C to +125°C
Lead Temperature (soldering, 10s) .... +300°C
Output Short Circuit Duration .... Continuous to Ground

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA102AG	16-Pin Ceramic DIP	109
INA102CG	16-Pin Ceramic DIP	109
INA102KP	16-Pin Plastic DIP	180
INA102AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
INA102AG	16-Pin Ceramic DIP	−25°C to +85°C
INA102CG	16-Pin Ceramic DIP	−25°C to +85°C
INA102KP	16-Pin Plastic DIP	0°C to +70°C
INA102AU	16-Pin Plastic SOIC	−25°C to +85°C

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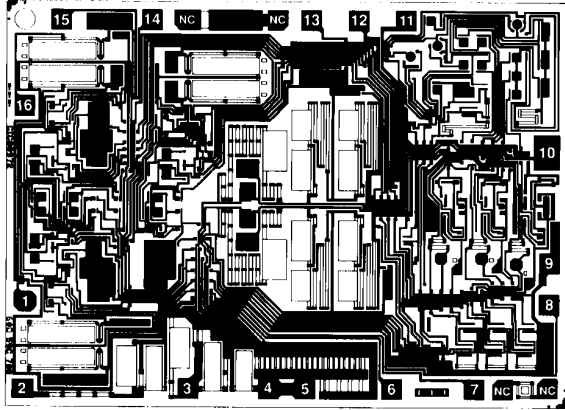
PAD	FUNCTION	PAD	FUNCTION
1	Offset Adjust	10*	Common
2	X10 Gain	11	Output
3	X100 Gain	12	$+V_{CC}$
4	X1000 Gain	13	Filter
5	X1000 Gain Sense	14	$-In$
6	Gain Sense	15	$+In$
7	Gain Set	16	Offset Adjust
8	CMR Trim	17	(A_1 Output)
9	$-V_{CC}$	18	(A_2 Output)

* Glass covers upper one-third of this pad.
Substrate Bias: Electrically connected to –V supply.
NC: No Connection.

INA102 DIE TOPOGRAPHY

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	142 x 104 ±5	3.61 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted.

COMMON-MODE REJECTION vs SOURCE IMBALANCE

GAIN vs FREQUENCY

COMMON-MODE REJECTION vs FREQUENCY

WARM-UP DRIFT vs TIME

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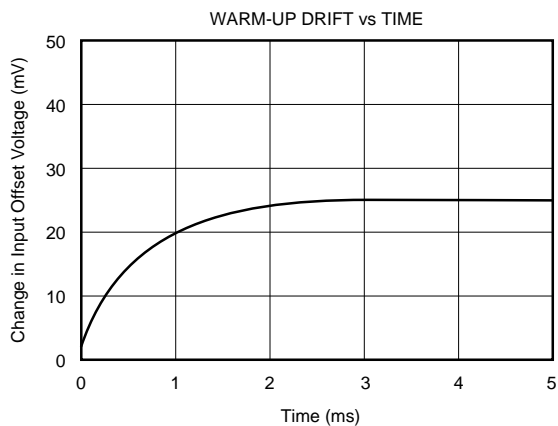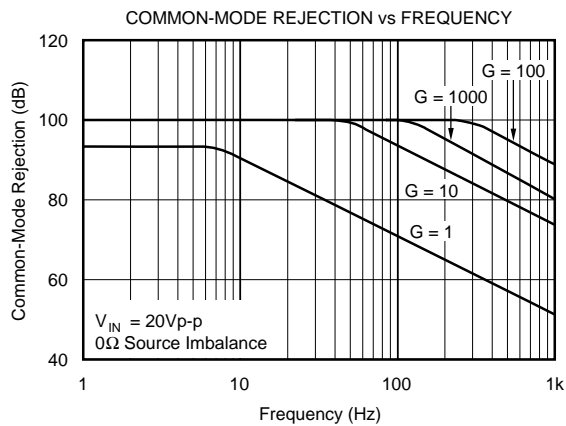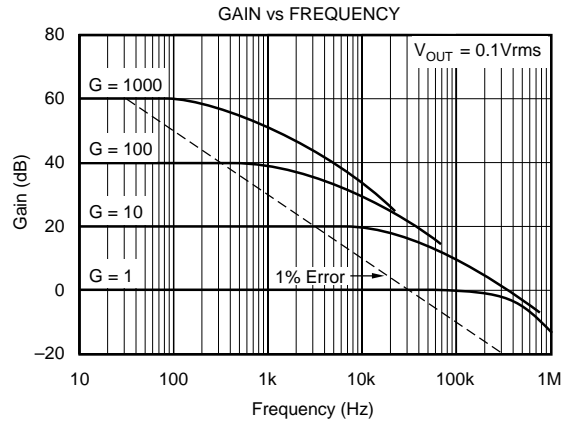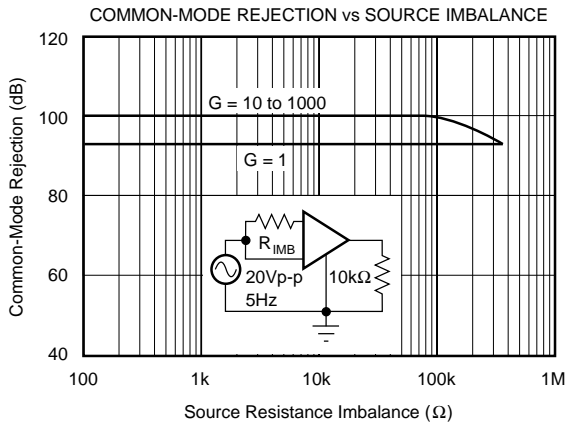
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C and in circuit of Figure 2 unless otherwise noted.

QUIESCENT CURRENT vs SUPPLY

$V_O = 10V$ (no load)

$V_O = 0$

Quiescent Current (μA) — Supply Voltage (V)

STEP RESPONSE

G = 1

G = 1000

$R_L = 10k\Omega$
$C_L = 1000pF$

Output Voltage (V) — Time (ms)

SETTLING TIME vs GAIN

$R_L = 10k\Omega$
$C_L = 1000pF$

0.01%

1%

0.1%

Settling Time (ms) — Gain (V/V)

PEAK-PEAK VOLTAGE NOISE vs GAIN

Bandwidth = 1Hz to 1MHz

500kΩ

500kΩ

R_S

$R_S = 1M\Omega$

$R_S = 100k\Omega$

$R_S = 0$

See Applications Section

Total Input Preferred Noise Voltage (μVp-p) — Gain (V/V)

INPUT NOISE VOLTAGE vs FREQUENCY

G = 1

G = 10

G = 100, G = 1000

Input Noise Voltage (nV√Hz) — Frequency (Hz)

POWER SUPPLY REJECTION vs FREQUENCY

Gain = 1000

Gain = 100

Gain = 10

Gain = 1

Power Supply Rejection (dB) — Frequency (Hz)

DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential-input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. The feedback networks of this instrumentation amplifier are included on the monolithic chip. No external resistors are required for gains of 1, 10, 100, and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design tradeoffs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high-input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems associated with op amps.

$$e_O = e_A + e_B$$
$$e_A = G(e_2 - e_1) = Ge_D$$
$$e_B = \frac{G(e_2 + e_1)/2}{CMRR} = \frac{Ge_{CM}}{CMRR}$$
$$e_O = Ge_D + \frac{Ge_{CM}}{CMRR}$$

Gain set is pin-programmable for x1, x10, x100, x1000 in the INA102.
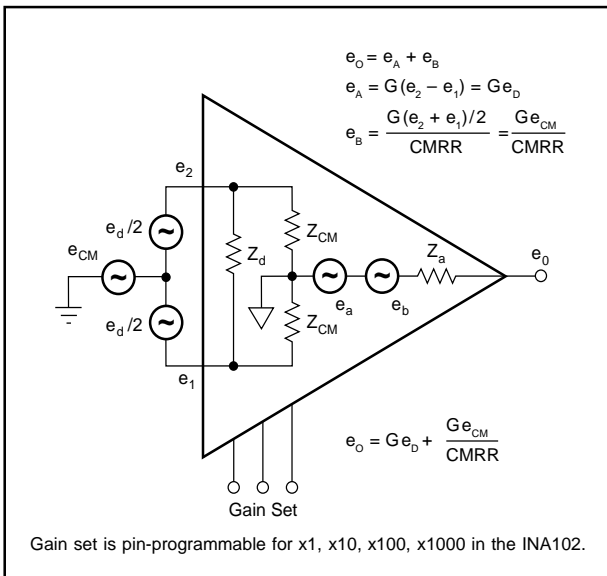
FIGURE 1. Model of an Instrumentation Amplifier.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, INA102 has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A_1 and A_2) incorporate high performance, low-drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input

impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage, and offset voltage versus temperature, are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A_3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

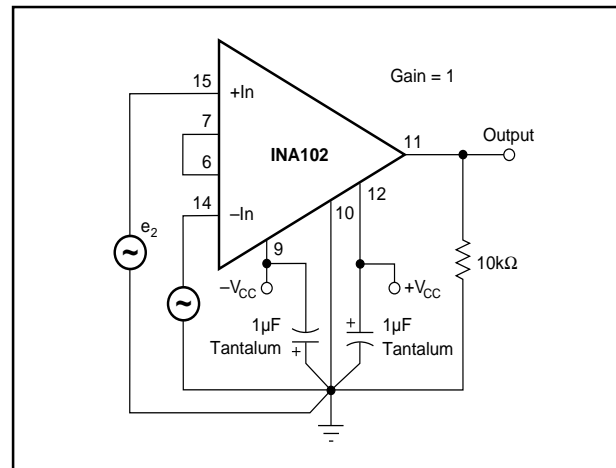TABLE I. Pin-Programmable Gain Connections.

FIGURE 2. Basic Circuit Connection for the INA102.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31µV/°C per 100µV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.
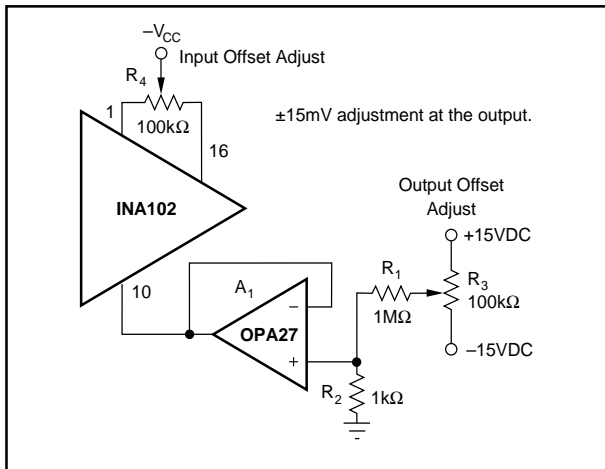
FIGURE 3. Optional Offset Nulling.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies, or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with some degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly, to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either positive or negative resistance value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.
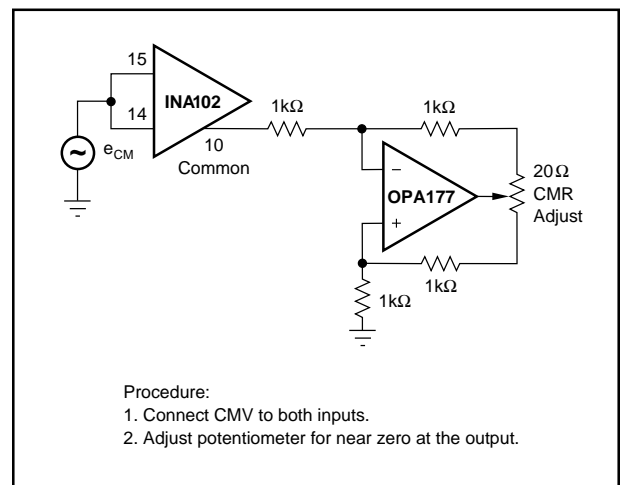

FIGURE 4. Optional Circuit for Externally Trimming CMR.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low quiescent current. However, in higher gains (>100), the bias current can cause a large offset error at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input. Figures 5 through 16 show some typical applications circuits.
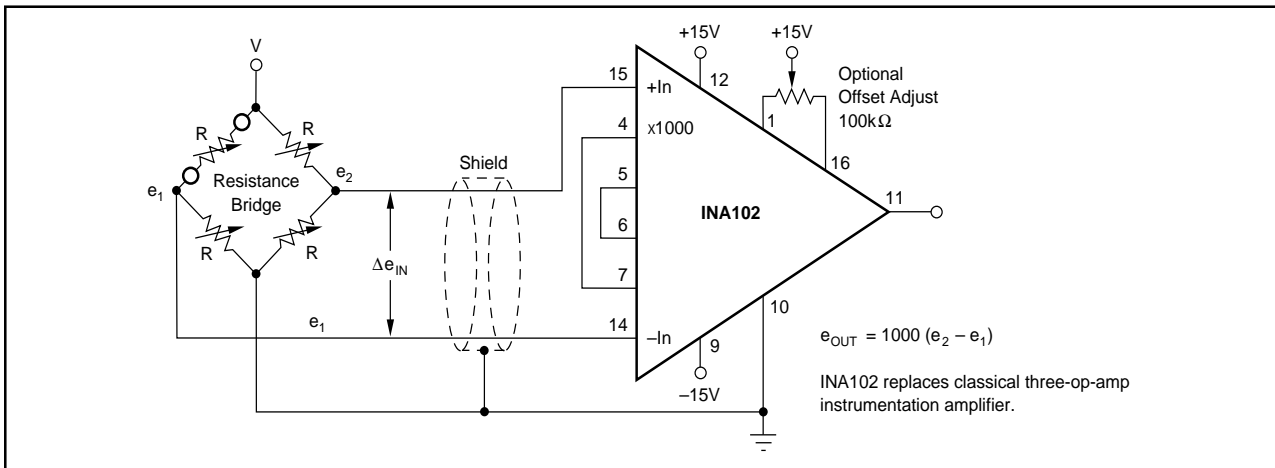
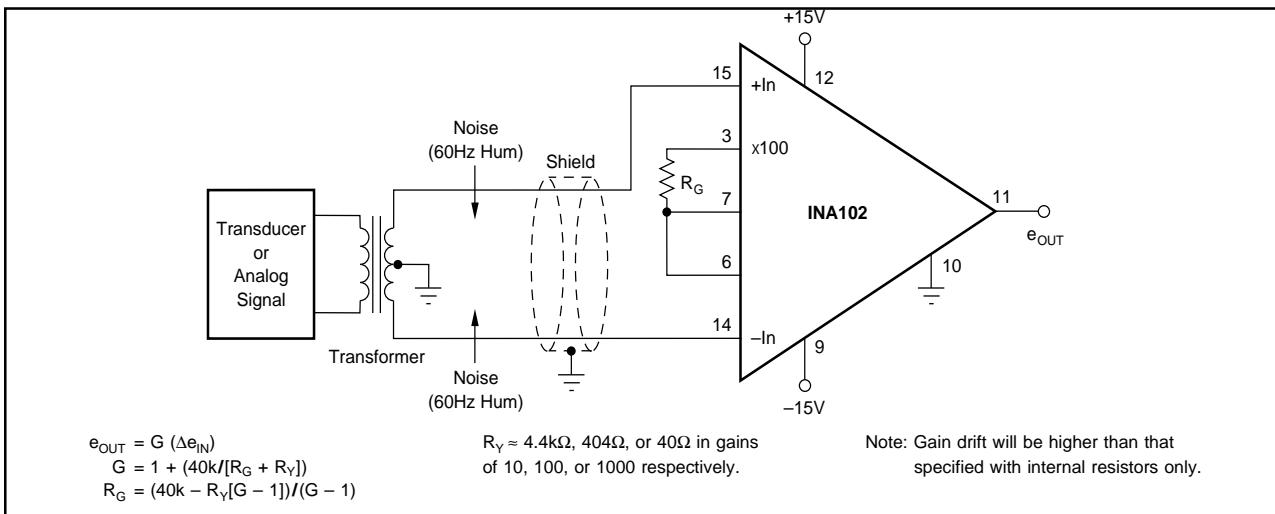FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

$e_{OUT} = G (\Delta e_{IN})$
$G = 1 + (40k/[R_G + R_Y])$
$R_G = (40k - R_Y[G - 1])/(G - 1)$

$R_Y \approx 4.4k\Omega$, 404Ω, or 40Ω in gains of 10, 100, or 1000 respectively.

Note: Gain drift will be higher than that specified with internal resistors only.

FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.
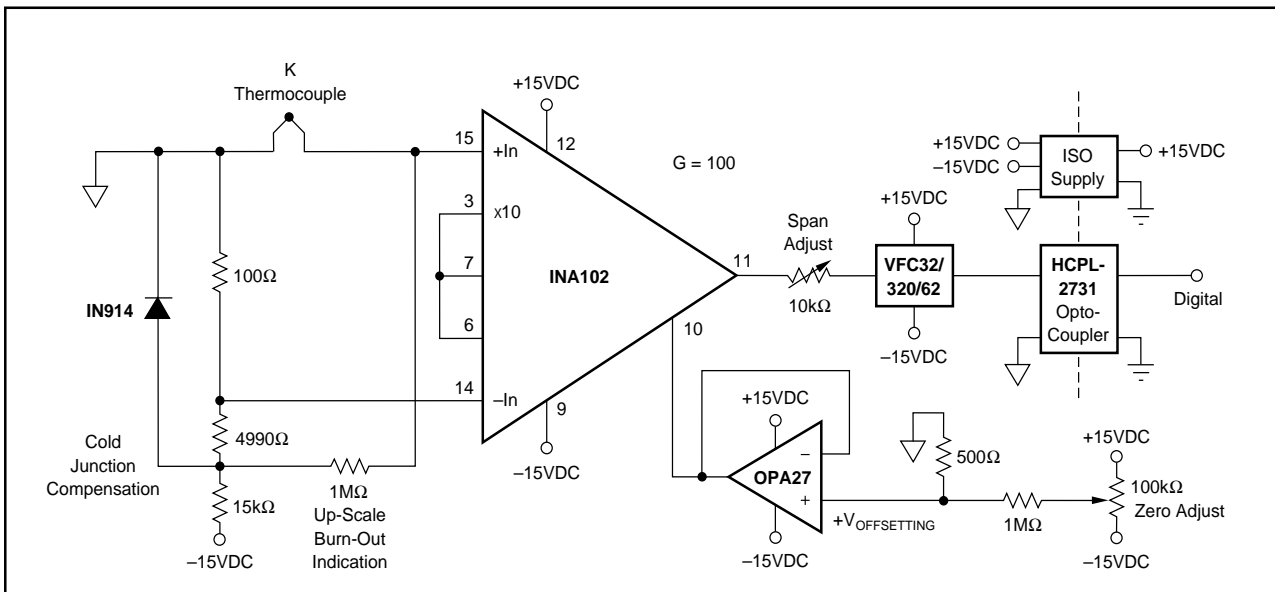
FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

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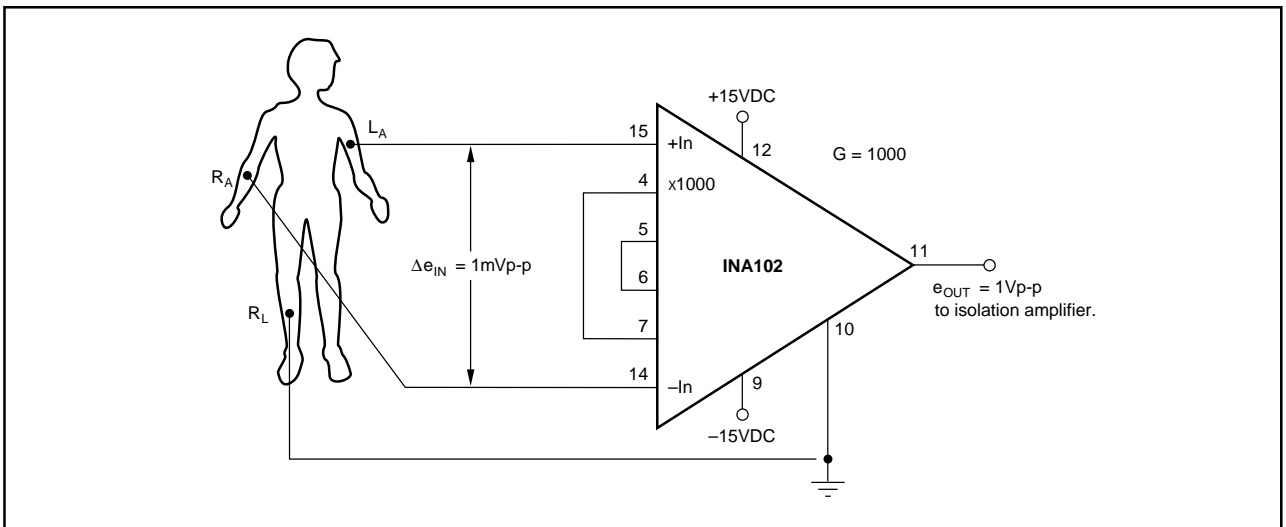
FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.
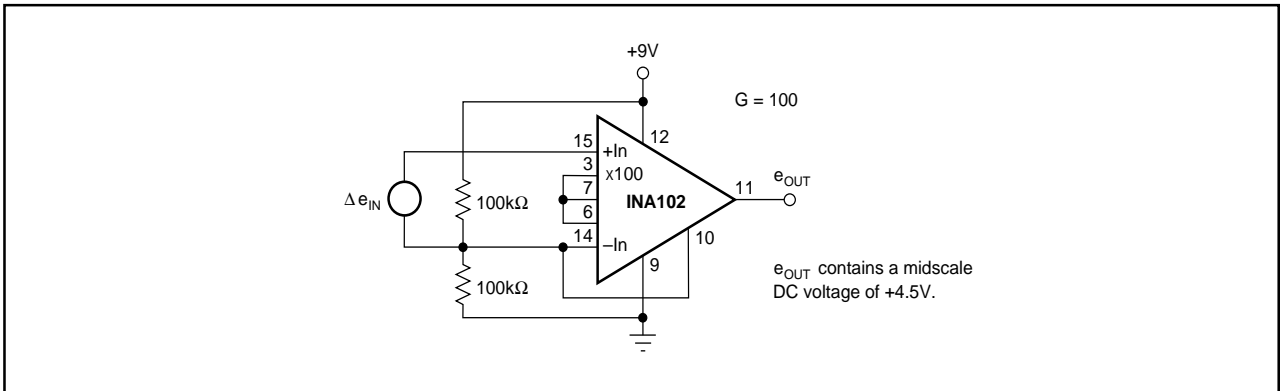
FIGURE 9. Single Supply Low Power Instrumentation Amplifier.
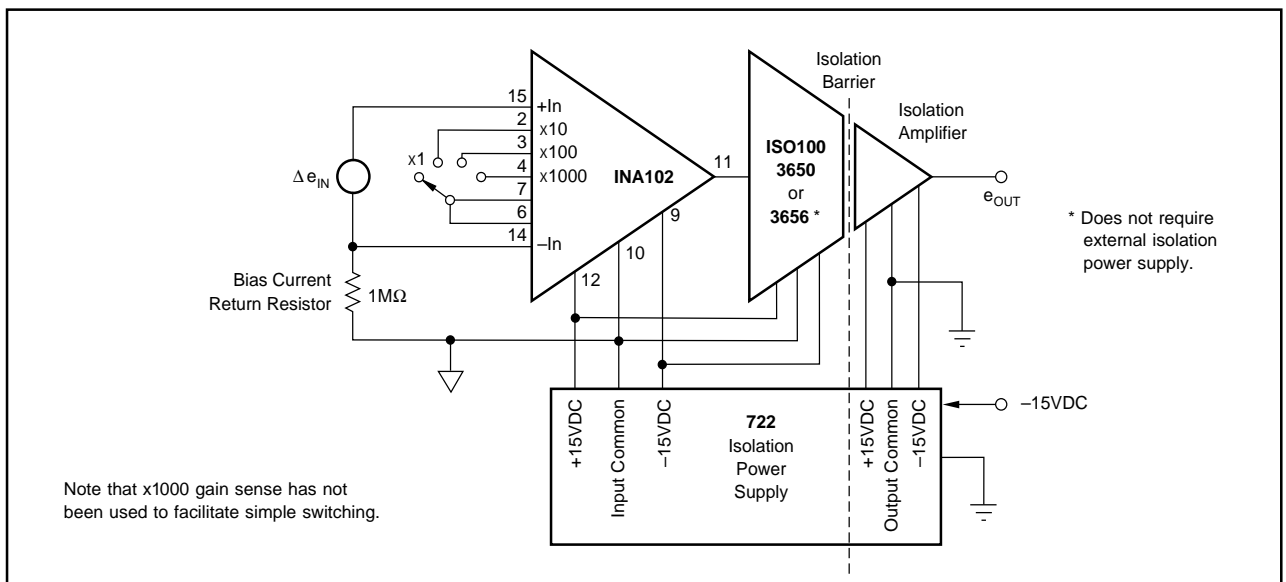
FIGURE 10. Precision Isolated Instrumentation Amplifier.
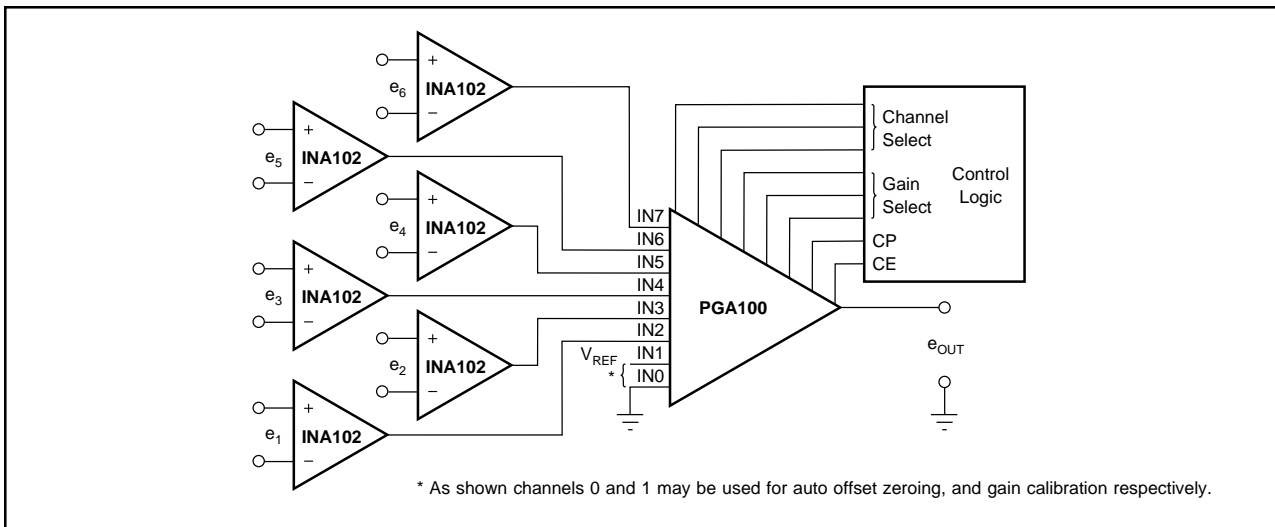
FIGURE 11. Multiple Channel Precision Instrumentation Amplifier with Programmable Gain.
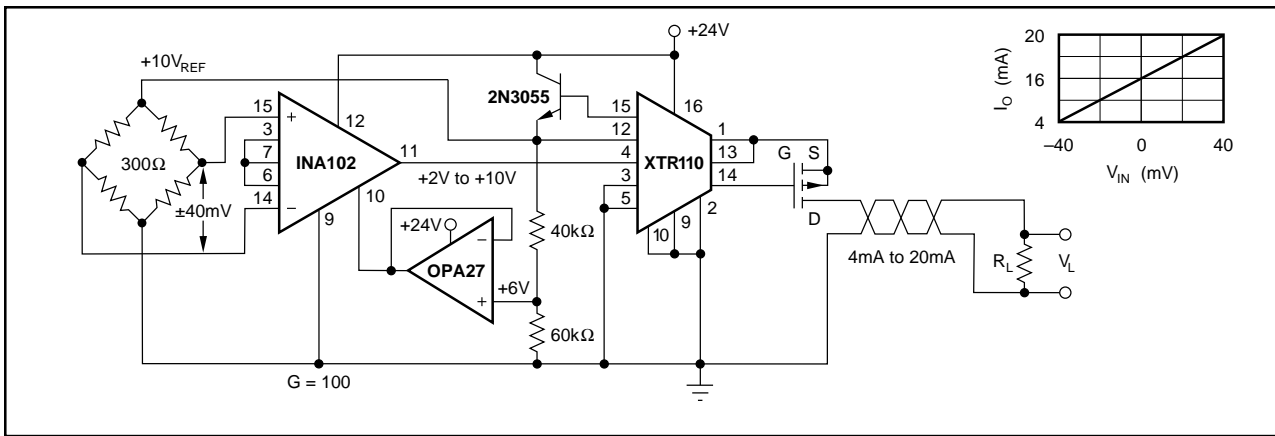
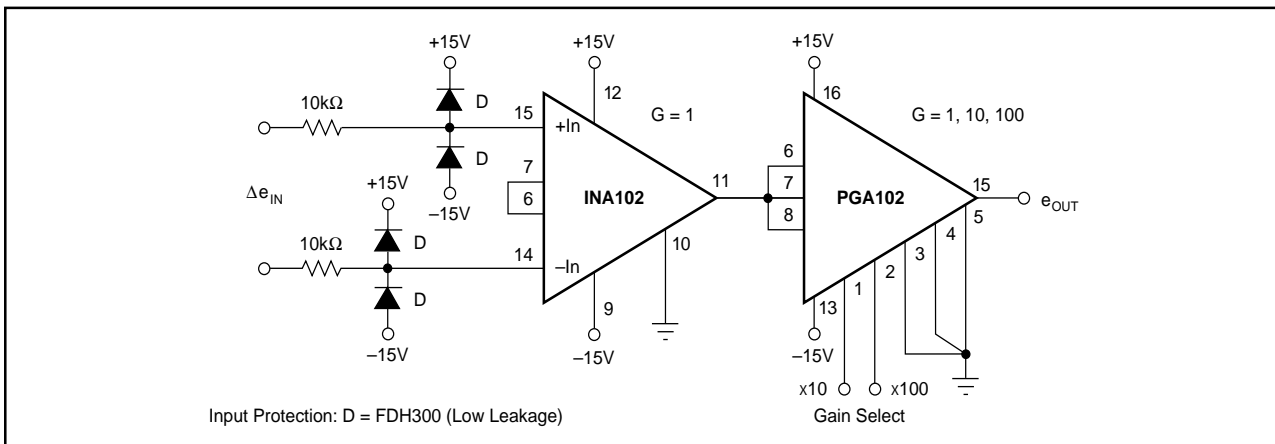FIGURE 12. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

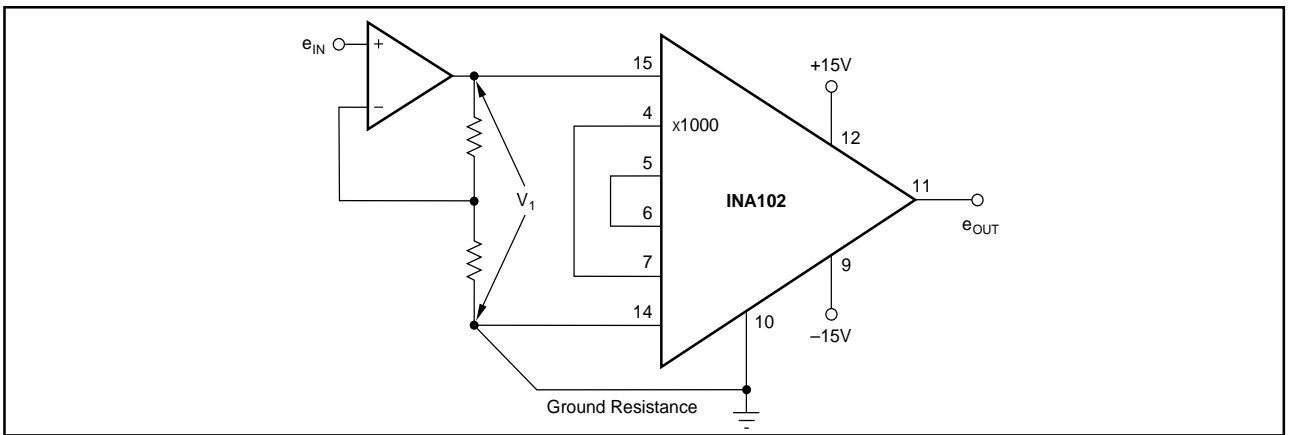FIGURE 13. Programmable-Gain Instrumentation Amplifier Using the INA102 and PGA102.

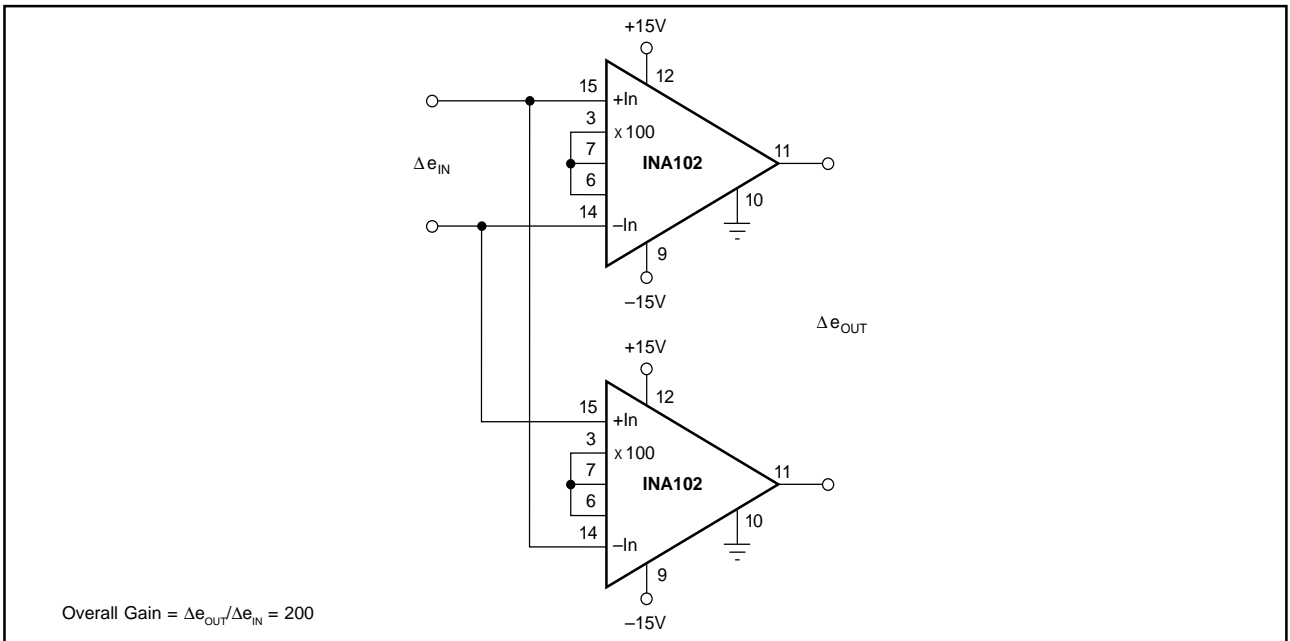FIGURE 14. Ground Resistance Loop Eliminator (INA102 senses and amplifies V_1 accurately).

Overall Gain = $\Delta e_{OUT}/\Delta e_{IN}$ = 200

FIGURE 15. Differential Input/Differential Output Amplifier (twice the gain of one INA).

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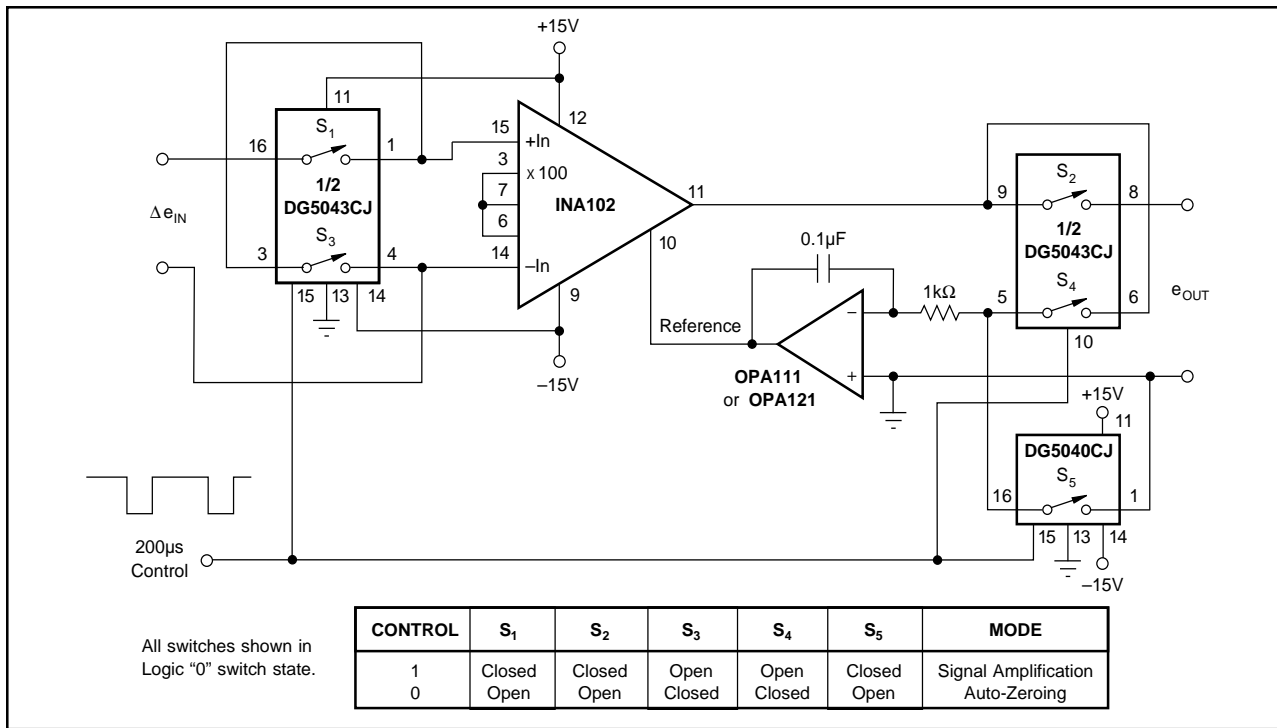
FIGURE 16. Auto-Zeroing Instrumentation Amplifier Circuit.

CONTROL	S_1	S_2	S_3	S_4	S_5	MODE
1	Closed	Closed	Open	Open	Closed	Signal Amplification
0	Open	Open	Closed	Closed	Open	Auto-Zeroing

All switches shown in Logic "0" switch state.