XTR110

SBOS141A – JANUARY 1984 – REVISED AUGUST 2003

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

APPLICATIONS

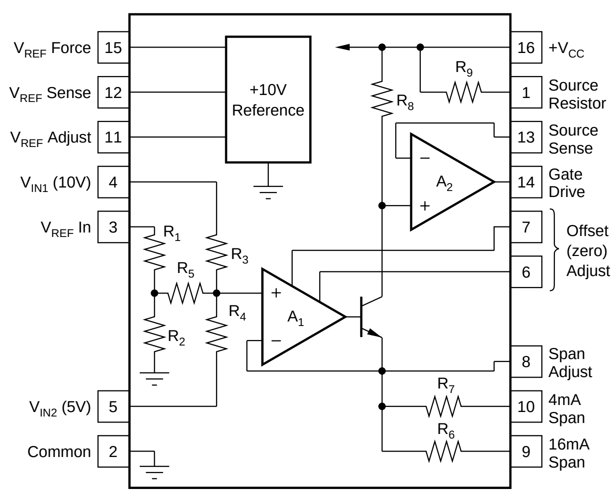
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4 to 20mA, 0 to 20mA, 5 to 25mA and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.



SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω**, unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AG, KP, KU			XTR110BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSMITTER								
Transfer Function		$I_O = 10\ [(V_{REF}In/16) + (V_{IN1}/4) + (V_{IN2}/2)]\ /R_{SPAN}$						
Input Range: V_{IN1}(5)	Specified Performance	0		+10	*		*	V
V_{IN2}	Specified Performance	0		+5	*		*	V
Current, I_O	Specified Performance(1)	4		20	*		*	mA
	Derated Performance(1)	0		40	*		*	mA
Nonlinearity	16mA/20mA Span(2)		0.01	0.025		0.002	0.005	% of Span
Offset Current, I_{OS}	I_O = 4mA(1)							
Initial	(1)		0.2	0.4		0.02	0.1	% of Span
vs Temperature	(1)		0.0003	0.005		*	0.003	% of Span/°C
vs Supply, V_{CC}	(1)		0.0005	0.005		*	*	% of Span/V
Span Error	I_O = 20mA							
Initial	(1)		0.3	0.6		0.05	0.2	% of Span
vs Temperature	(1)		0.0025	0.005		0.0009	0.003	% of Span/°C
vs Supply, V_{CC}	(1)		0.003	0.005		*	*	% of Span/V
Output Resistance	From Drain of FET (Q_{EXT})(3)		10×10^9			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} In		19			*		kΩ
Dynamic Response								
Settling Time	To 0.1% of Span		15			*		µs
	To 0.01% of Span		20			*		µs
Slew Rate			1.3			*		mA/µs
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temperature			35	50		15	30	ppm/°C
vs Supply, V_{CC}	Line Regulation		0.0002	0.005		*	*	%/V
vs Output Current	Load Regulation		0.0005	0.01		*	*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range		–0.100		+0.25	*		*	V
Output Current	Specified Performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4.5		*	*	mA
TEMPERATURE RANGE								
Specification: AG, BG		–40		+85	*		*	°C
KP, KU		0		+70				°C
Operating: AG, BG		–55		+125	*		*	°C
KP, KU		–25		+85				°C

* Specifications same as AG/KP grades. ** Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by ($+V_{CC}$ – 2V) $+V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 3. (5) For extended I_{REF} drive circuit see Figure 4. (5) Unit may be damaged. See section, "Input Voltage Range".

ABSOLUTE MAXIMUM RATINGS

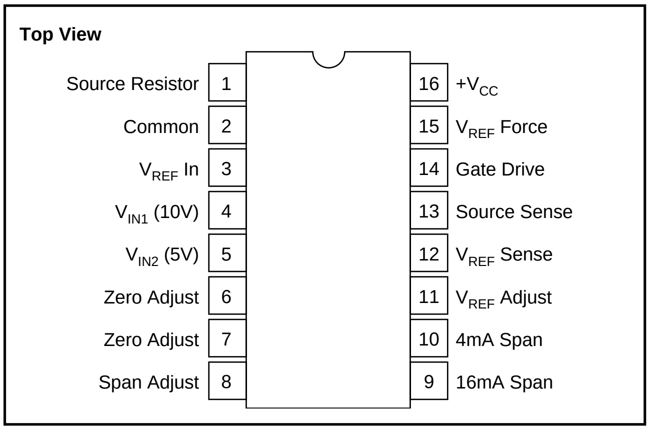
Power Supply, $+V_{CC}$ 40V
Input Voltage, V_{IN1}, V_{IN2}, $V_{REF\ IN}$ .... $+V_{CC}$
See text regarding safe negative input voltage range.
Storage Temperature Range: A, B .... –55°C to +125°C
K, U .... –40°C to +85°C
Lead Temperature
(soldering, 10s) G, P .... 300°C
(wave soldering, 3s) U .... 260°C
Output Short-Circuit Duration, Gate Drive
and V_{REF} Force .... Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor 40mA

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
XTR110AG	16-Pin Ceramic DIP	109
XTR110BG	16-Pin Ceramic DIP	109
XTR110KP	16-Pin Plastic DIP	180
XTR110KU	SOL-16 Surface-Mount	211

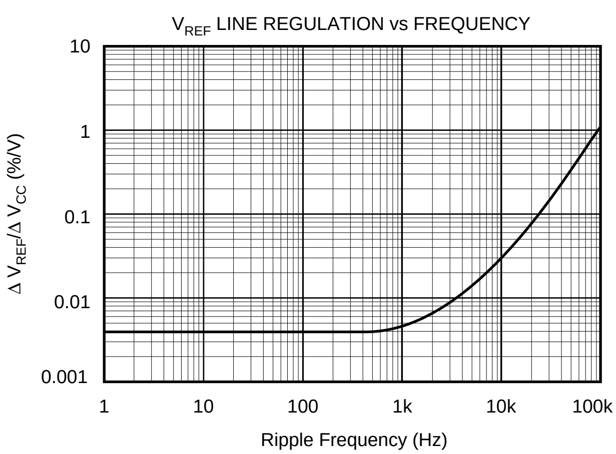
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

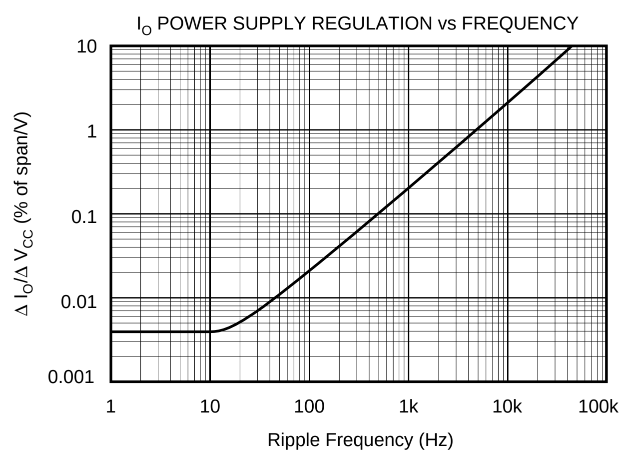
ORDERING INFORMATION

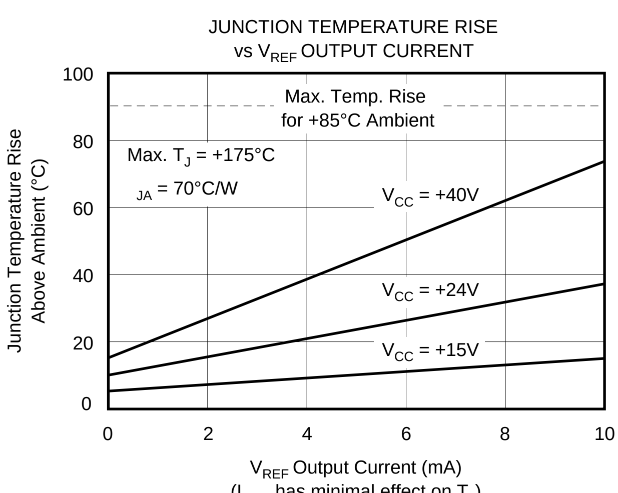
PRODUCT	PACKAGE	TEMPERATURE RANGE
XTR110AG	16-Pin Ceramic DIP	–40°C to +85°C
XTR110BG	16-Pin Ceramic DIP	–40°C to +85°C
XTR110KP	16-Pin Plastic DIP	0°C to +70°C
XTR110KU	SOL-16 Surface-Mount	0°C to +70°C

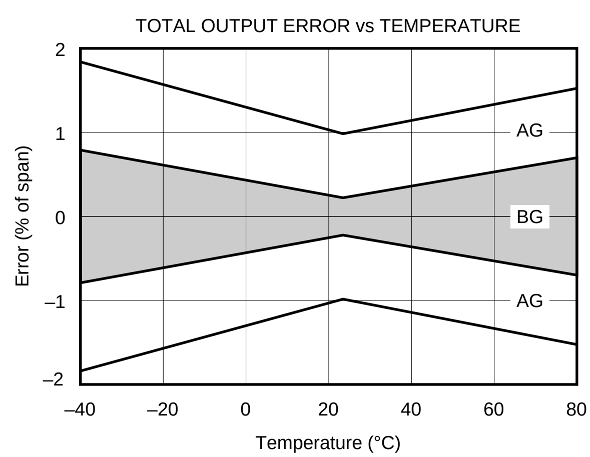
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω, unless otherwise noted.









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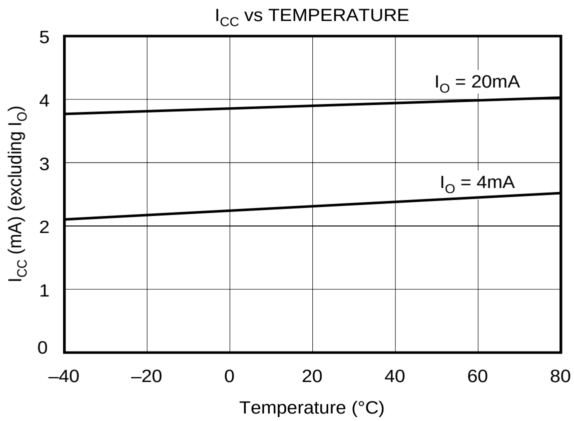
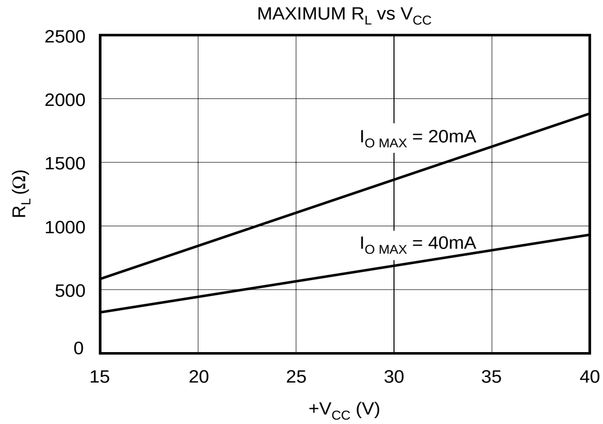
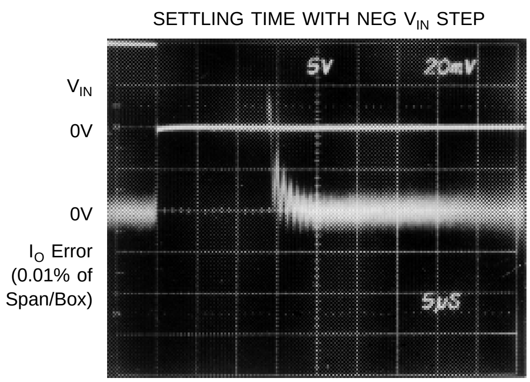
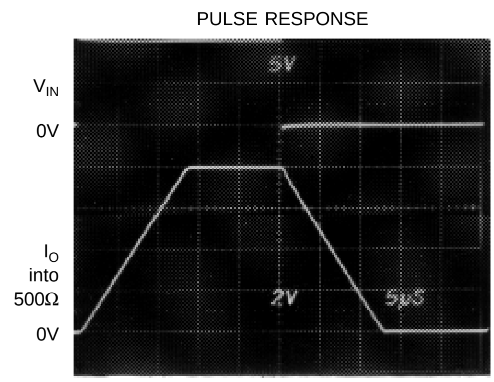
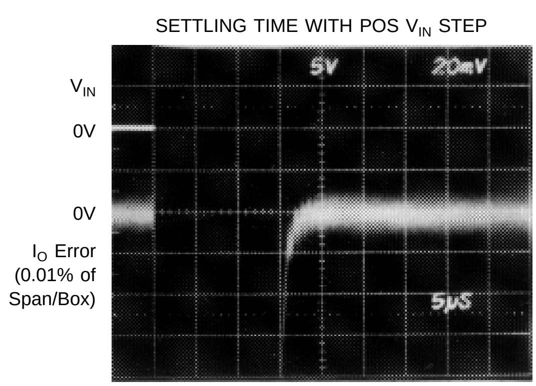










APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for 0 to 10V input and 4 to 20mA output. Other input voltage and output current ranges require changes in connections of pins 3, 4, 5, 9 and 10 as shown in the table of Figure 1.

The complete transfer function of the XTR110 is:

$$I_O = \frac{10\left[\frac{(V_{REF\ IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2}\right]}{R_{SPAN}} \qquad (1)$$

R_{SPAN} is the internal 50Ω resistor, R_9, when connected as shown in Figure 1. An external R_{SPAN} can be connected for different output current ranges as described later.

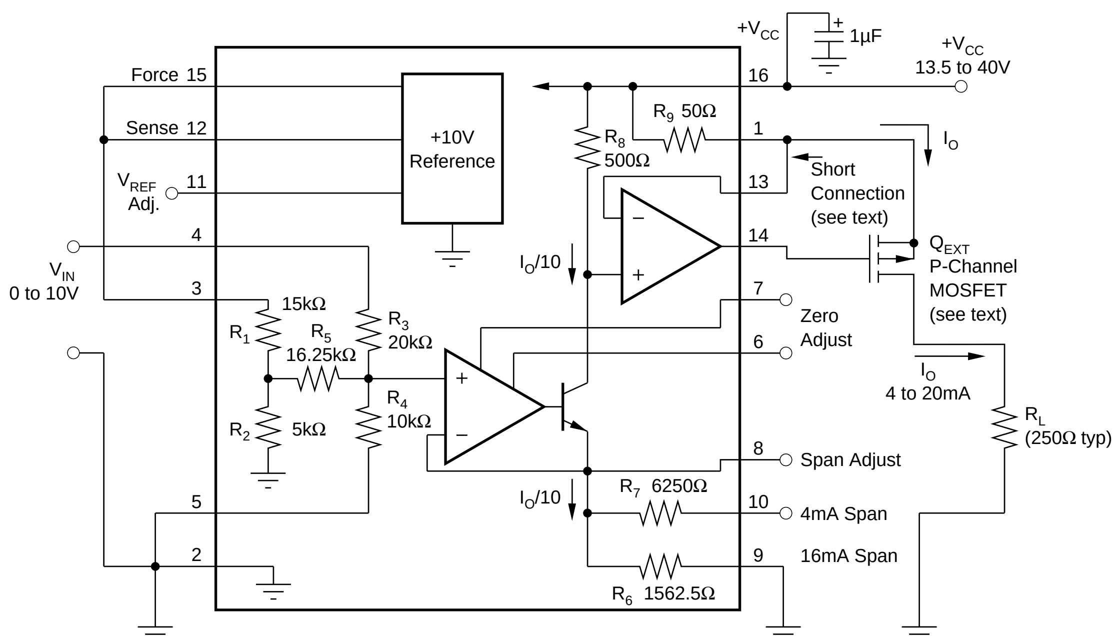
EXTERNAL TRANSISTOR

An external pass transistor, Q_{EXT}, is required as shown in Figure 1. This transistor conducts the output signal current. A P-channel MOSFET transistor is recommended. It must have a voltage rating equal or greater than the maximum power supply voltage. Various recommended types are shown in Table I.

MANUFACTURER	PART NO.	BV_{DSS}(1)	BV_{GS}(1)	PACKAGE
Ferranti	ZVP1304A	40V	20V	TO-92
	ZVP1304B	40V	20V	TO-39
	ZVP1306A	60V	20V	TO-92
	ZVP1306B	60V	20V	TO-39
International Rectifier	IRF9513	60V	20V	TO-220
Motorola	MTP8P08	80V	20V	TO-220
RCA	RFL1P08	80V	20V	TO-39
	RFT2P08	80V	20V	TO-220
Siliconix (preferred)	VP0300B	30V	40V	TO-39
	VP0300L	30V	40V	TO-92
	VP0300M	30V	40V	TO-237
	VP0808B	80V	40V	TO-39
	VP0808L	80V	40V	TO-92
	VP0808M	80V	40V	TO-237
Supertex	VP1304N2	40V	20V	TO-220
	VP1304N3	40V	20V	TO-92
	VP1306N2	60V	20V	TO-220
	VP1306N3	60V	20V	TO-92

NOTE: (1) BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

TABLE I. Available P-Channel MOSFETs.



INPUT RANGE (V)	OUTPUT RANGE (mA)	PIN 3	PIN 4	PIN 5	PIN 9	PIN 10
0-10	0-20	Com	Input	Com	Com	Com
2-10	4-20	Com	Input	Com	Com	Com
0-10	4-20	+10V Ref	Input	Com	Com	Open
0-10	5-25	+10V Ref	Input	Com	Com	Com
0-5	0-20	Com	Com	Input	Com	Com
1-5	4-20	Com	Com	Input	Com	Com
0-5	4-20	+10V Ref	Com	Input	Com	Open
0-5	5-25	+10V Ref	Com	Input	Com	Com

FIGURE 1. Basic Circuit Connection.

If the supply voltage, $+V_{CC}$, exceeds the gate-to-source breakdown voltage of Q_{EXT}, and the output connection (drain of Q_{EXT}) is broken, Q_{EXT} could fail. If the gate-to-source breakdown voltage is lower than $+V_{CC}$, Q_{EXT} can be protected with a 12V zener diode connected from gate to source.

Two PNP discrete transistors (Darlington-connected) can be used for Q_{EXT}—see Figure 2. Note that an additional capacitor is required for stability. Integrated Darlington transistors are not recommended because their internal base-emitter resistors cause excessive error.

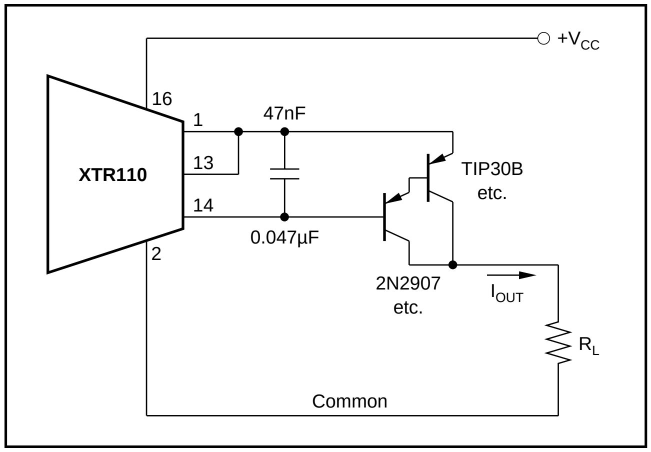


FIGURE 2. Q_{EXT} Using PNP Transistors.

TRANSISTOR DISSIPATION

Maximum power dissipation of Q_{EXT} depends on the power supply voltage and full-scale output current. Assuming that the load resistance is low, the power dissipated by Q_{EXT} is:

$$P_{MAX} = (+V_{CC})\ I_{FS} \quad (2)$$

The transistor type and heat sinking must be chosen according to the maximum power dissipation to prevent overheating. See Table II for general recommendations.

PACKAGE TYPE	ALLOWABLE POWER DISSIPATION
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Use if hermetic package is required.

TABLE II. External Transistor Package Type and Dissipation.

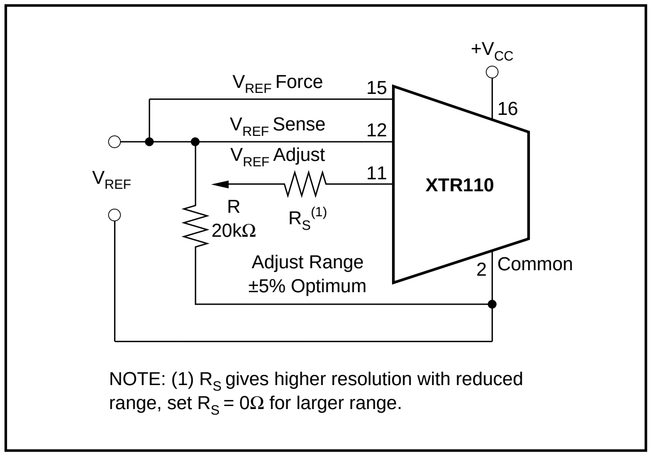


FIGURE 3. Optional Adjustment of Reference Voltage.

INPUT VOLTAGE RANGE

The internal op amp A_1 can be damaged if its non-inverting input (an internal node) is pulled more than 0.5V below common (0V). This could occur if input pins 3, 4 or 5 were driven with an op amp whose output could swing negative under abnormal conditions. The voltage at the input of A_1 is:

$$V_{A1} = \frac{(V_{REF\ IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \quad (3)$$

This voltage should not be allowed to go more negative than –0.5V. If necessary, a clamp diode can be connected from the negative-going input to common to clamp the input voltage.

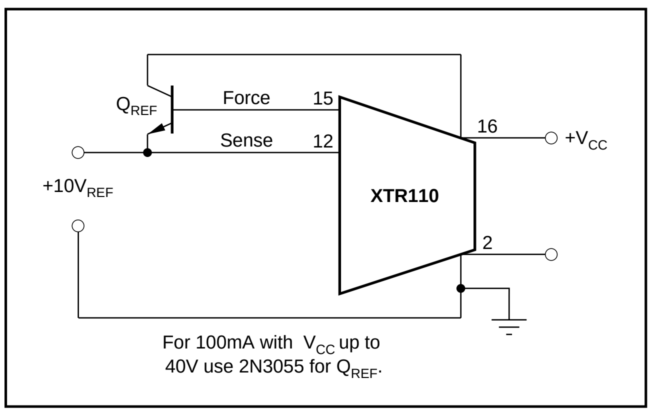


FIGURE 4. Increasing Reference Current Drive.

COMMON (Ground)

Careful attention should be directed toward proper connection of the common (grounds). All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any point where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 ($V_{REF\ SENSE}$). To preserve accuracy, any load including pin 3 should be connected to this point. The circuit in Figure 3 shows adjustment of the voltage reference.

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 4.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. Set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting

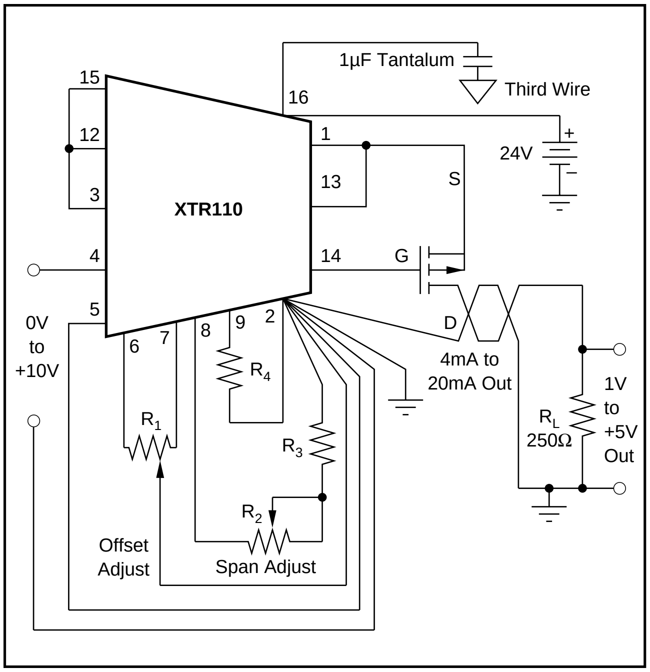


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

LOW TEMPERATURE COEFFICIENT OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient (TC) of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the output current can have 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

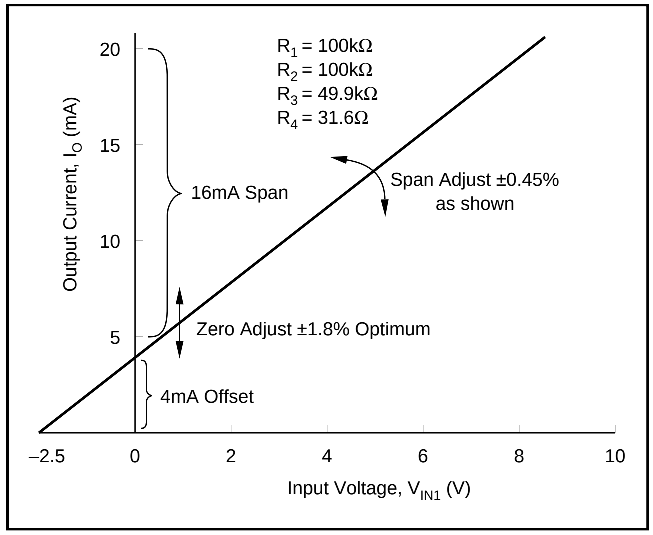


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

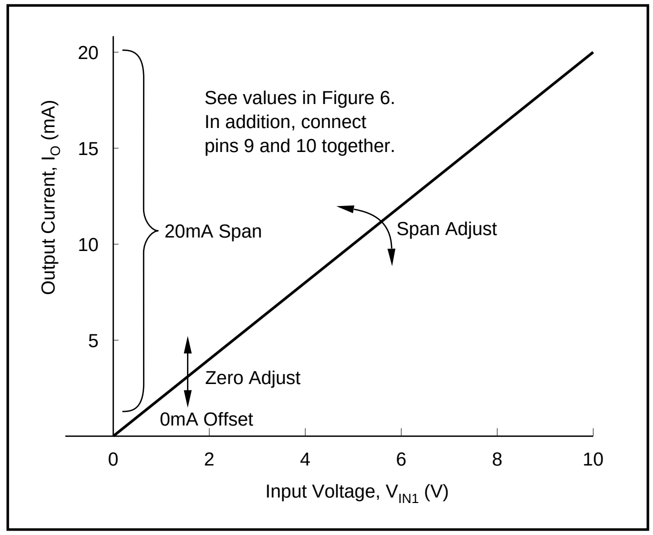


FIGURE 7. Zero and Span of 0V to $+10V_{IN}$, 0mA to 20mA Output Configuration (see Figure 5).

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

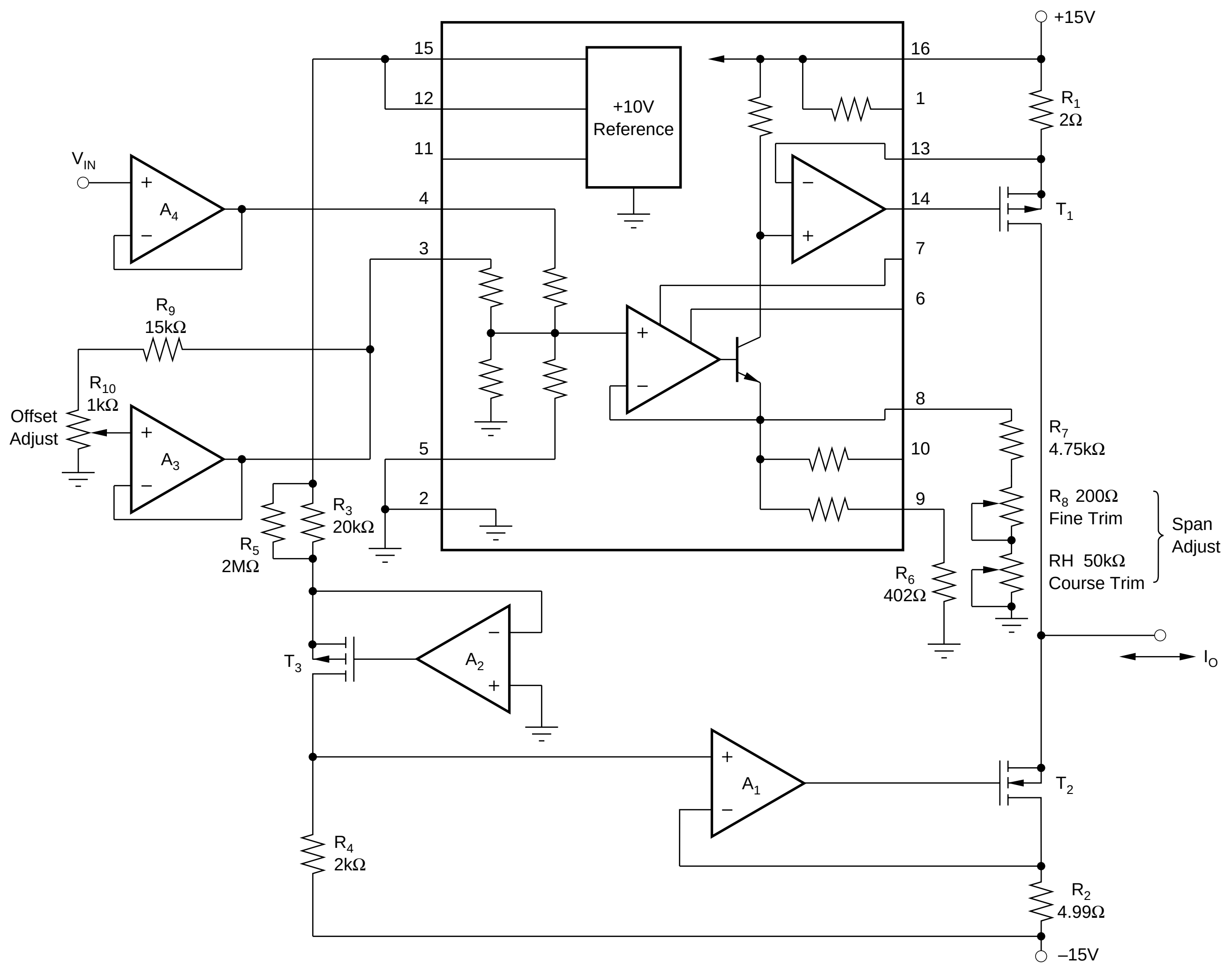
$$R_{EXT} = R_9\ (Span_{OLD}/Span_{NEW})$$

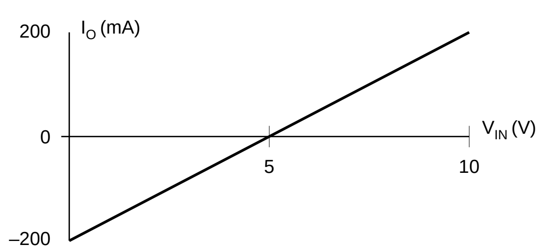
Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 10 for application.

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference can be used to excite bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 8 through 10 show typical applications of the XTR110.





R_1, R_2: Low TC resistors to dissipate 0.32W continuous power.
For other current ranges, scale both resistors proportionately.
R_8, R_{10}, R_{11}: 10-turn trimpots for greatest sensitivity.
R_6, R_7: Low TC resistors.
A_1 - A_4: 1/4 LM324 (powered by ±15V).
T_1: International Rectifier IR9513(1).
T_2: International Rectifier IR513(1).
T_3: International Rectifier IRFF9113(1).

NOTE: (1) Or other adequate power rating MOS transistor.

FIGURE 8. ±200mA Current Pump.

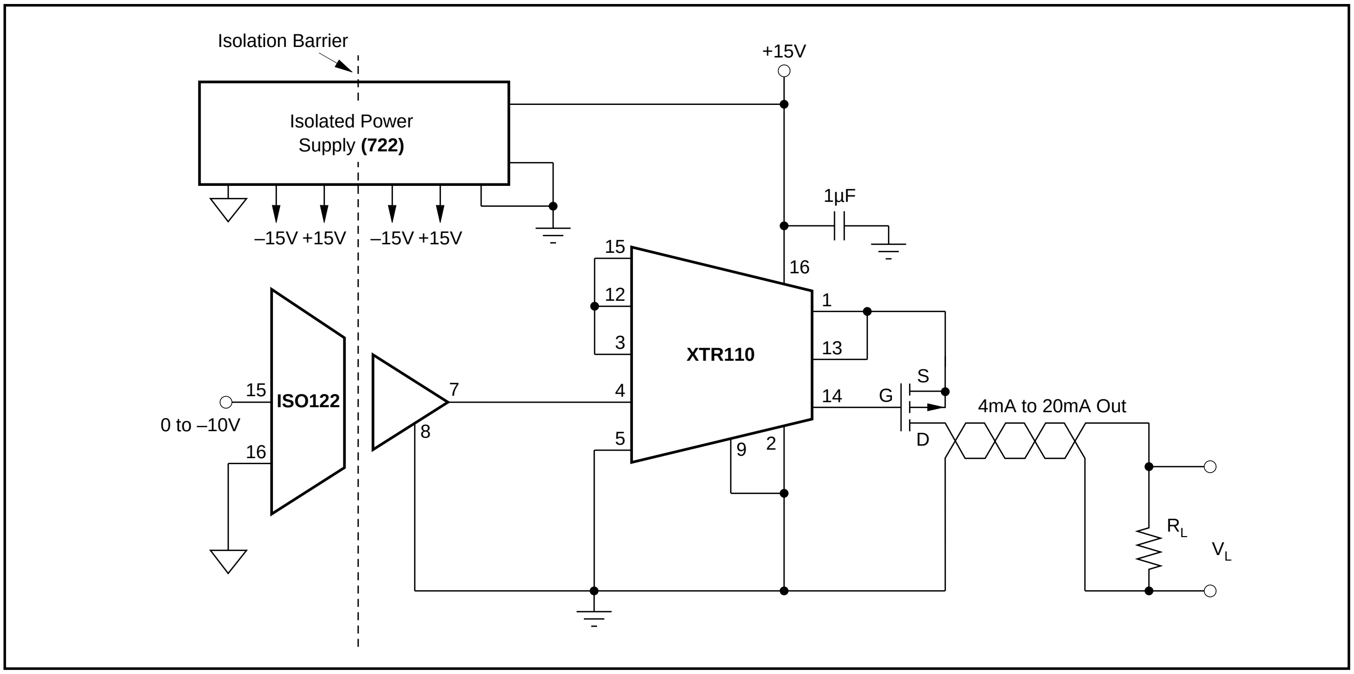


FIGURE 9. Isolated 4mA to 20mA Channel.

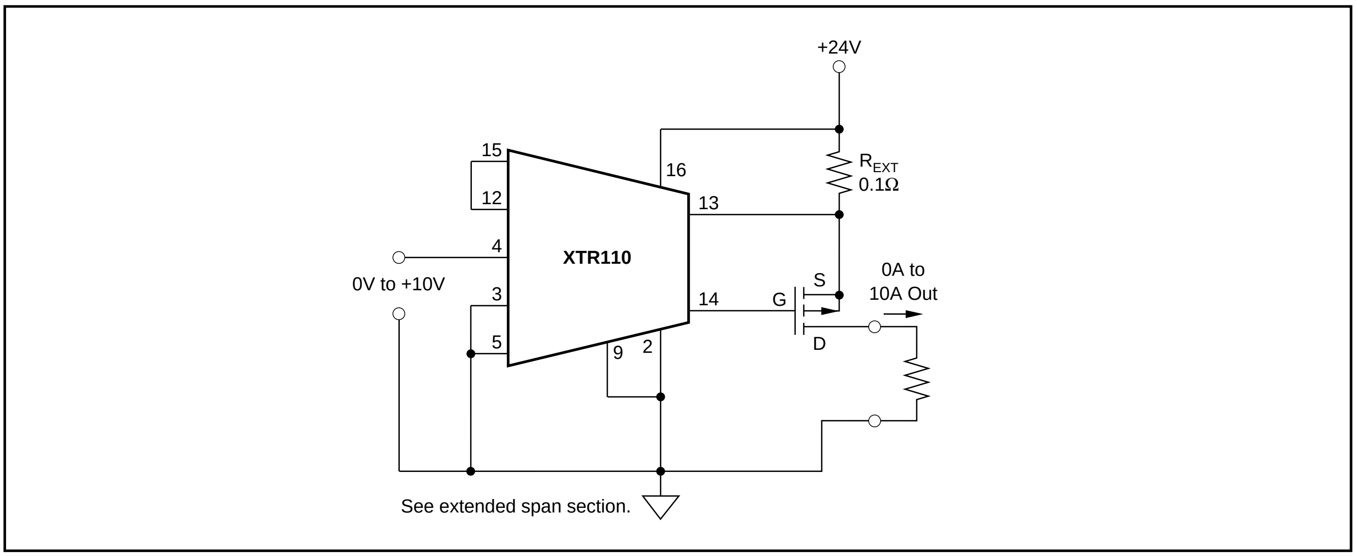
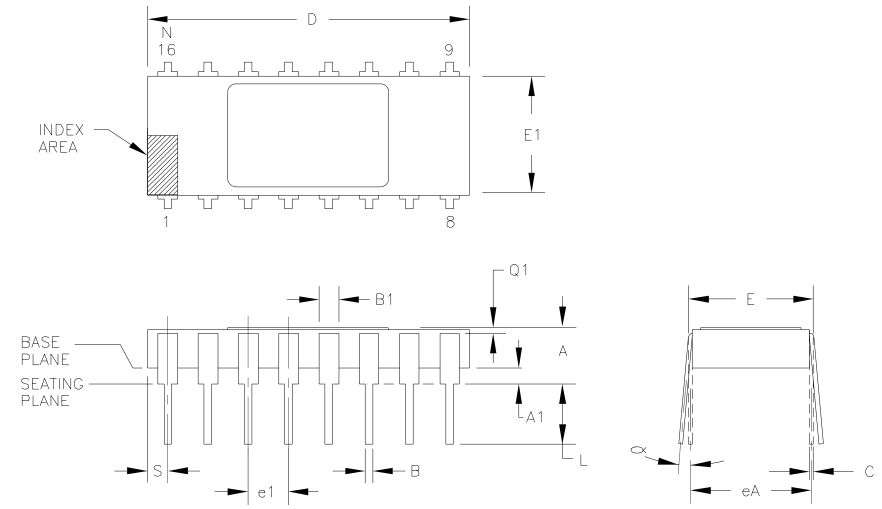


FIGURE 10. 0A to 10A Output Voltage-to-Current Converter.

Package Number 109 - 16-Lead, Ceramic Side Braze DIP, .300 Wide



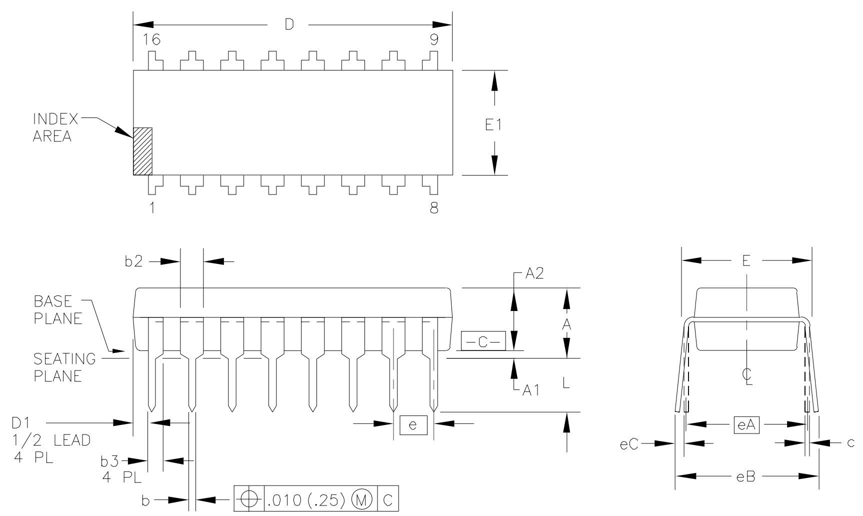
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45		∝	0°	15°	0°	15°	3
A1	.025	.055	0.64	1.40							
B	.015	.021	0.38	0.53	5						
B1	.038	.060	0.97	1.52	5						
C	.008	.012	0.20	0.30							
D	.770	.830	19.56	21.08							
E	.290	.325	7.37	8.26							
E1	.280	.310	7.11	7.87	6						
e1	.100 TYP.		2.54 TYP.		2						
eA	.300 TYP.		7.62 TYP.		2						
L	.125	.175	3.18	4.45							
N	16		16		4						
Q1	.010	--	0.25	--							
S	.020	.065	0.51	1.65							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ109	REV.:	D
JEDEC NUMBER: MO–36–AD		

Package Number 180 - 16-Pin Plastic, Single-Wide DIP



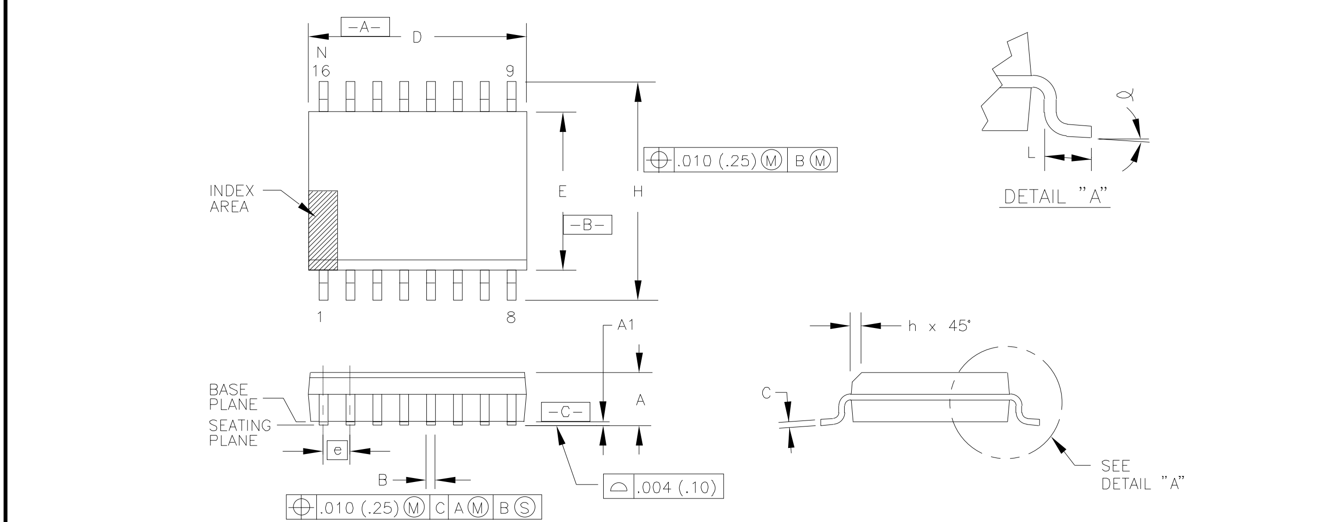
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	eC	.000	.060	0.00	1.52	6
A1	.015	--	0.38	--	3	L	.115	.150	2.92	3.81	3
A2	.115	.195	2.92	4.95		N	16		16		7
b	.014	.022	0.36	0.56							
b2	.045	.070	1.14	1.78	9						
b3	.030	.045	0.76	1.14	9						
c	.008	.014	0.20	0.36							
D	.735	.775	18.67	21.34	4						
D1	.005	--	0.13	--	4						
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.63 BASIC		5						
eB	--	.430	--	10.92	6						

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM –C– .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS D0 NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ180	REV.:	F
JEDEC NUMBER: MS–001–BB		

Package Number 211 - 16-Lead SOIC, .300 Wide



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.3977	.4133	10.10	10.50	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	16		16		6
∝	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. L IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. N IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH B, AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ211	REV.: F
JEDEC NUMBER: MS-013-AA	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
XTR110AG	NRND	CDIP SB	JD	16	24	None	Call TI	Level-NA-NA-NA
XTR110BG	NRND	CDIP SB	JD	16	24	None	Call TI	Level-NA-NA-NA
XTR110KP	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	Call TI	Level-NC-NC-NC
XTR110KU	ACTIVE	SOIC	DW	16	48	None	CU NIPDAU	Level-2-220C-1 YEAR
XTR110KU/1K	ACTIVE	SOIC	DW	16	1000	None	CU SNPB	Level-2-220C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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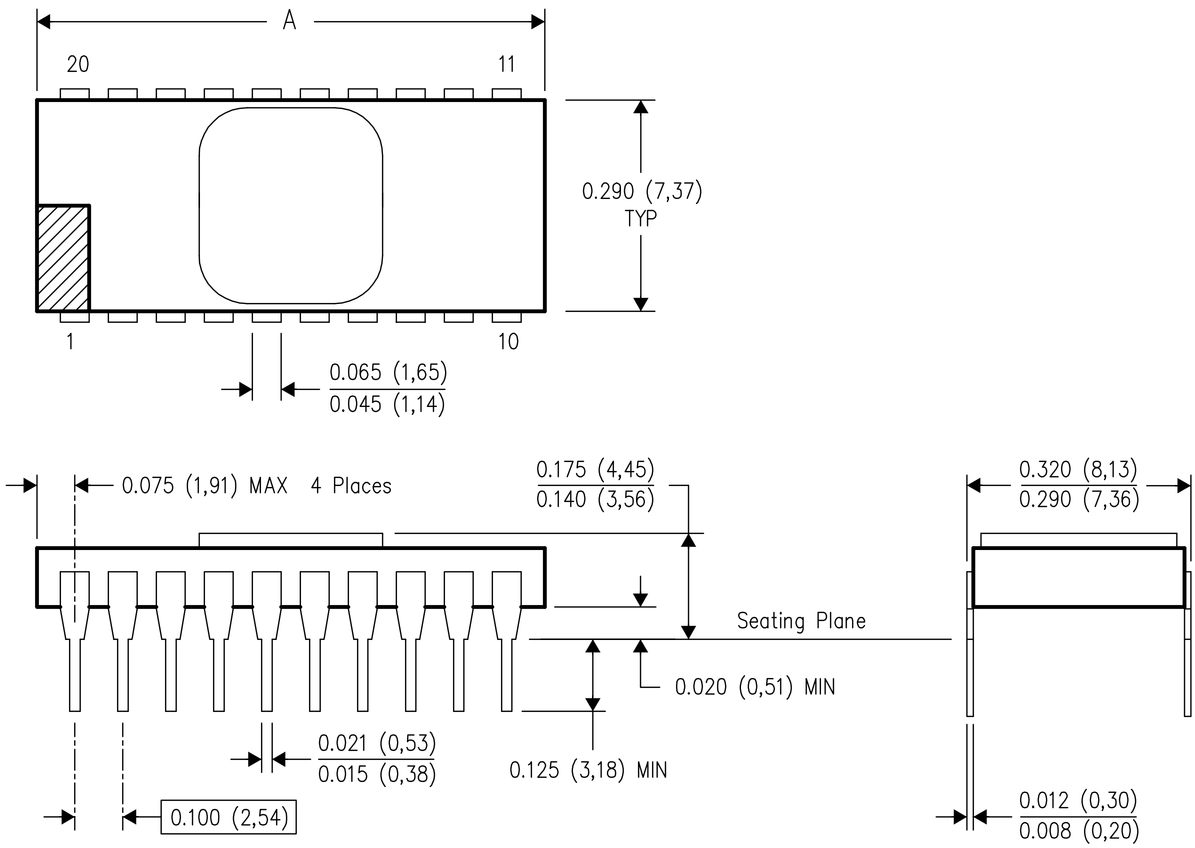
JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

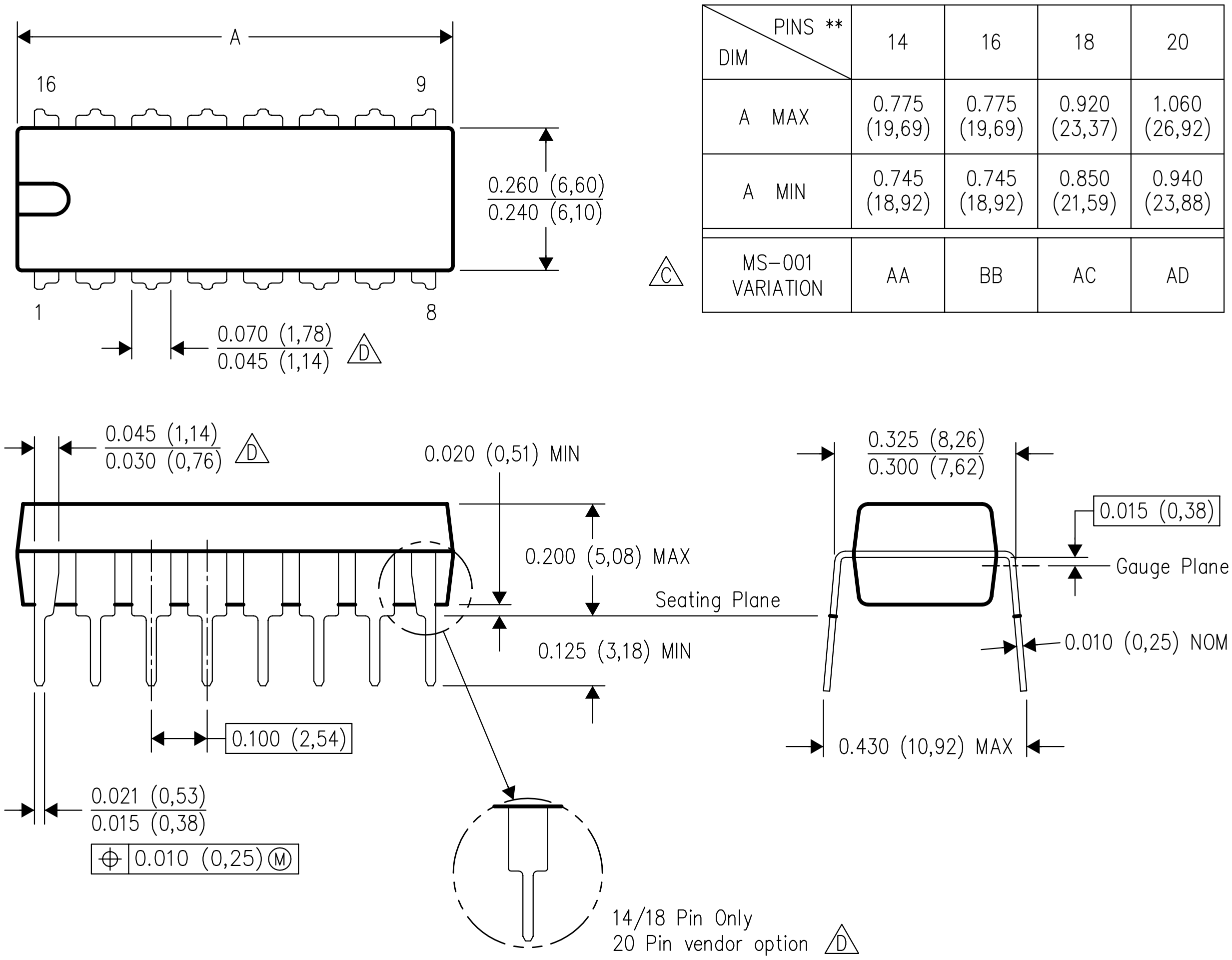
4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

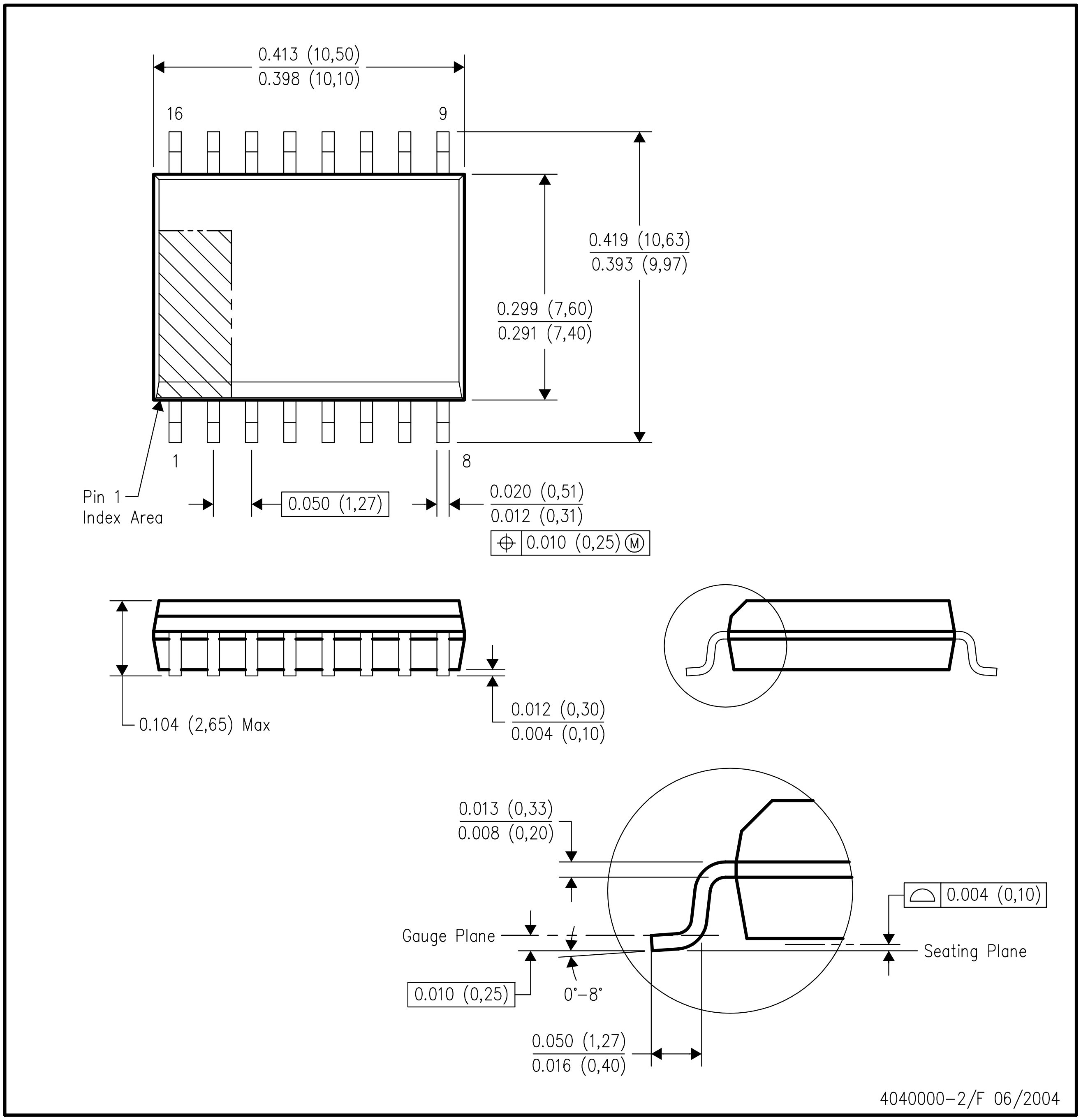
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.