PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

A Calculating Device

We, VEB ELEKTRONISCHE RECHENMASCHINEN-WISSENSCHAFTLICHER INDUSTRIEBETRIEB-KARL-MARX-STADT, of 219, Zwickauer Strasse, Karl-Marx-Stadt, W.30, Eastern Germany, a National Corporation organised under the laws of Eastern Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to calculating devices for the addition or subtraction of two decimal numbers, the individual digits of which are represented in the four-digit binary code, that is to say four binary digits are used to represent a decimal digit. A group of four binary digits will be referred to hereinafter for convenience as a tetrade.

More particularly, the invention relates to binary decimal calculating devices which are designed to operate in accordance with the serial mode, that is to say that the binary digits of the tetrades to be processed are supplied in succession to the calculating device from a store, and the digits of the result tetrade are likewise supplied in succession to a store.

Since ten decimal digits have to be represented by binary digits at least groups of four digits (tetrades) have to be used as is well known. On the other hand, four digits give 16 possible combinations of which only 10 are required for the representation of the ten decimal digits. In carrying out additions or subtractions, it then may happen that the result tetrade does not represent a decimal digit, that is to say it is one of the six tetrades which are not employed for the representation of a decimal digit (which tetrade will be referred to hereinafter a pseudo-decimals) and therefore provision must be made for a correction of the result tetrade if it happens to be a pseudo-decimal. If a four digit binary code is used in which each decimal digit is represented by the corresponding binary number, then the six tetrades representing decimal numbers greater than nine are pseudo-decimals. Therefore, provision must be made for a correction of the result tetrade when this tetrade is a pseudo-decimal.

There are known calculating devices which effect a correction when a pseudo-decimal results. The present invention is concerned with an improved calculating device of this kind.

The invention consists in a serial calculating device for the addition or subtraction of two decimal numbers the individual digits of which are coded in a binary four-digit code, which calculating device comprises a main adder-subtractor to which the individual four-digit groups (tetrades) of the two decimal numbers are supplied in succession and in serial mode, a correction adder-subtractor which receives the output from the said main adder-subtractor and the required correction tetrade to produce their algebraic sum, the output from the said main adder-subtractor being added into or subtracted from the correction adder-subtractor according to whether the said two decimal numbers are being added or subtracted respectively, and a selector unit, which depending on whether correction was necessary or not, selects for further processing the tetrade issued by the main adder-subtractor or the tetrade issued by the correction adder-subtractor.

These features of the calculating device according to the invention and additional features of two preferred embodiments thereof will now be described in detail with reference to the accompanying drawings, in which

Figure 1 shows by way of a block diagram one embodiment of a calculating device according to the invention;

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Figure 2 represents the circuit of a known adder-subtractor suited to be used in the calculating device according to Figure 1;

Figure 3 represents a known shift register for use in the arrangement shown in Figure 1;

Figure 4 shows in more detail the circuit arrangement of the calculating device according to Figure 1;

Figure 5 shows by way of a block diagram another embodiment of a calculating device according to the invention;

Figure 6 shows an embodiment of a simplified correction circuit for addition;

Figure 7 shows an extension of the correction device for subtraction;

Figure 8 shows the arrangement of a known and-circuit;

Figure 9 shows the arrangement of a known or-circuit.

Two 4-unit binary decimal digits (tetrades) x_1 and x_2 have to be added or subtracted. The decimal digits are coded directly in a 4-unit binary code, that is to say in the form $z_i=x_i$ (z_i is a decimal digit, x_i is the same digit represented in binary form, that is to say as powers of two). Figure 1 shows how the two terms run from two cyclic-store tracks 1 and 2 into an adder-subtractor 3, the augend to the adder input 4 and the addend to the adder input 5. In subtraction, the minuend goes to input 4 and the subtrahend to input 5. The result leaving the adder at output 6 is fed to a shift register 7 and to a correction adder subtractor 8 through its input 10. A correction tetrade, for instance OLLO=6, is supplied to the adder-subtractor to the adder-substractor 8 via its input 9. The sum leaving the correction adder via output 11 passes to a shift register 12. A correction decider 13 checks the sum tetrade to see whether it has to be corrected or not, and influences a selector 14 which selects either the corrected or the uncorrected sum tetrade. The adder 3 and the correction adder 8 may, for example, be pure binary adders as shown in Figure 2. The sum of two binary digits is given by the logical expression $a \cdot \bar{b} + \bar{a} \cdot b$ wherein $\cdot$ is the symbol for a conjunction (And-circuit), $+$ the symbol for a disjunction (Or-circuit), $\bar{b}$ the symbol for the inversion of b (negator).

Two And-circuits 15 and 16 in Figure 2, which are represented by empty circles, and an Or-circuit 17, which is represented by a circle which is filled in in black, provide the partial sum S_1 of the binary terms a and b. The conjunctions $\bar{a} \cdot b$ and $a \cdot \bar{b}$ may also be used to form the carry in subtraction. Both the partial sum S_1 and its inverted value $\bar{S}_1$ are needed. The inverted partial sum $\bar{S}_1$ is obtained from the partial sum S_1 by interposing the negator 18. Figure 2. As regards the circuit symbols shown, it should be added that the output of the individual logical circuits is always designated by a dot. The carry $\ddot{u}_{n-1}$ the preceding digit place must also be added to the partial sum S_1 of the two binary numbers. Thus the final binary digit of the sum is given by the logical expression

$$S=S_1 \cdot \overline{\ddot{u}_{n-1}} + S_1 \cdot \ddot{u}_{n-1}$$

$\ddot{u}_{n-1}$ being the carry from the preceding digit place. The carry may, for example, be supplied by the carry flip-flop 19 which delays the carry by one binary place. In subtraction the sum S is formed in precisely the same way, but the carry is produced differently. Two control lines 20 and 21 give the instruction as to whether adding or subtraction is to be carried out. For addition, the control line 20 conveys a signal L corresponding to the binary one and the control line 21 conveys a signal O corresponding to the binary zero. In subtraction it is the reverse. When the control line 20 conveys the signal L, the conjunction $a \cdot b$ switches on the carry flip flop, and only switches it off again for $\bar{a} \cdot \bar{b}$. For this purpose the conjunctions $20 \cdot a \cdot b$ and $20 \cdot \bar{a} \cdot \bar{b}$ are provided. When the control line 21 conveys the signal L, the conjunction $21 \cdot \bar{a} \cdot b$ switches the carry flip-flop on and the conjunction $21 \cdot a \cdot \bar{b}$ switches it off again. The two And-circuits 22 and 23 for each flip-flop position on the one hand and the And-circuits 24 and 25 on the other hand are combined through Or-circuit 26 or 27 and connected to the switching input of a pulse gate 28 and 29 respectively. If the signal L is applied to the input of the gates and if, as an additional condition, the synchronizing pulse s reaches the gate through the input indicated by an arrow, then the associated flip-flop side, which is connected to the output of the gate characterised by the dot, is set to L. The synchronizing pulse s appears at the beginning of each binary digit period and so initiates the digit signals L or O.

As an example of an embodiment of a shift register or delay line, Figure 3 shows a known flip-flop chain 34 and 35 which is stepped or through pulse gates 30, 31, 32 or 33 by means of synchronizing pulses s. These pulses are very brief and only last for a fraction of the digit period. Each synchronizing pulse s transfers the contents of the preceding flip-flop into the following one. Accordingly, if the flip-flop 34 delivers a signal of the value L at its output 36 and the flip-flop 35 has a signal of the value O at its output 37, the

inverting outputs $\overline{36}$ and $\overline{37}$ deliver the signals O and L respectively. An O is supplied to the input of the delay-line with $\overline{38}$=O or $\overline{38}$=L at the required instant of the binary digit period. Thus, the gates 31 and 32 are open for the synchronizing pulse *s* at the end of this binary digit period, since a signal L appears only at their switching inputs. The synchronizing pulse *s* switches the flip-flop 34 off and the flip-flop 35 on, as a result of which the value L moves on by one member.

For an understanding of the whole circuit shown in Figure 4, it must first be explained when correction has to be effected and what value has to be added or subtracted. With direct coding, a correction is always necessary when one of the following six pseudo-decimals occur

S_1	S_2	S_3	S_4
L	O	L	O
L	O	L	L
L	L	O	O
L	L	O	L
L	L	L	O
L	L	L	L

or a carry appears in the next following 4-unit signal tetrade. In addition, for example, OLOL+OLOL (5+5) will not give OOOO as the sum and OOOL as a carry into the next-higher place, but the pseudo-decimal ten=LOLO. In order to obtain the true value one (OOOL) and zero (OOOO), a binary "six" (OLLO) must be added. For example the addition of the tetrade nine gives an L as the sum tetrade and an L as a carry into the next following tetrade. The tetrade six (OLLO) must likewise be added. In subtraction, for example, seven minus nine gives a binary pseudo-decimal, namely fourteen= LLLO and a carry into the next place. Here a correction has to be carried out with minus "six" in order to obtain the correct value eight and a carry. The case where the subtrahend is greater than the minuend increased by six only produces a carry but no pseudo-decimal. Here, too, a correction must be made with minus six. Thus for subtraction, there is only one condition for correction in that a correction has to be carried out with minus six whenever a carry into the next 4-unit signal appears.

Figure 4 shows the two binary adder-subtractors; in the sum-producing adder the carry is produced in a manner somewhat differently from that of the correction adder-subtractor. The carry for the addition is formed in accordance with the logical equation

$$\ddot{u}_{n+}=a \cdot b \cdot 20+S_1 \cdot \ddot{u}_{n-1} \cdot 20$$

by two triple And-circuits 39 and 40 which are combined in an Or-circuit 41. For the carry in subtraction, the logical equation

$$\ddot{u}_{n-}=\overline{a} \cdot b \cdot 21+\overline{S_1} \cdot \ddot{u}_{n-1} \cdot 21$$

applies.

This gives the whole carry for addition and subtraction of

$$\ddot{u}_{n\,ges}=a \cdot b \cdot 20+\overline{a} \cdot b \cdot 21+S_1 \cdot \ddot{u}_{n-1} \cdot 20+\overline{S_1} \cdot \ddot{u}_{n-1} \cdot 21$$

which is realized by four And-circuits 39, 40, 42 and 43 which are combined in a four-input Or-circuit 41. These circuits may, for example, be known diode combinations as shown in Figures 8 and 9. Two And-circuits 42 and 43 for the carry are only in duplicate because $\overline{a} \cdot b$ and $\overline{S_1} \cdot \ddot{u}_{n-1}$ are already needed to find the sum.

The correction adder-subtractor is like the sum-producing adder-subtractor already described. A switching pulse train of such a form that the voltage wave assumes the value O during the period of two binary places is supplied from a pulse generator to the input 44 of the correction adder. This pulse sequence is produced in the control section by a pulse generator which is not illustrated because it is also needed for other units of the computer and so does not involve any additional expenditure. Furthermore, the two signals of value L have to occur during the period of the two centre digits in each tetrade from which it will be seen that the correction value six is fed constantly into the correction adder-subtractor, being added during addition but subtracted during sub-traction, as caused by the control through the inputs 20 and 21. Thus the correction adder is controlled in precisely the same manner as the main adder according to the operation in question. The sum representing tetrade is not only supplied to the correction adder but also to the shift register 7. The corrected sum tetrade is fed into the shift register 12. S_1, S_2, S_3 and S_4 are the four places of the sum tetrade (S_4 being the least significant place in this example), $\ddot{u}_n$ is the carry to the following tetrade supplied to the adder. Thus the correction decision is obtained through circuit embodiment of the logical equation:—

$$K_c=S_1 \cdot S_2+S_1 \cdot S_3+\ddot{u}_n \text{ (Correction decision)}$$
$$=S_1 \cdot (S_2+S_3)+\ddot{u}_n.$$

The term $S_1 \cdot S_2+S_1 \cdot S_3$ results from the pseudo-decimals, the term $\ddot{u}_{n-1}$ from the carry to the next order stage of the adder.

During addition, a carry into the next tetrade may result due to the addition of a six to the pseudo-decimal. If the next sum of tetrade is a nine, this carry may lead to the necessity for a fresh correction addition, because the pseudo-decimal ten=LOLO is obtained. In order to avoid that this carry produced in the correction adder separately added to the next tetrade, as is also necessary for values other than nine in the sum tetrade,

no carry is sent to the next tetrade from the correction adder. The pulse train $h_1+h_5+\ldots$ coming from the pulse generator which supplies a pulse at the beginning of each tetrade period then resets the carry flip-flop 45 in the correction adder. At the same time, if a carry was present, the carry flip-flop 48 of the main adder is set through a gate 46 by the pulse input 47 to which the mentioned pulse train is supplied. The signal $\ddot{u}_{n-1\,k}$, that is to say the carry into the next tetrade, lies at the control input 49 of the gate 46. From this it will be seen that the pulse train $h_1+h_5+\ldots$ does not coincide with the first synchronizing pulse s of each tetrade but appears somewhat later after the conditions switched by s have already been fully established. The h_1 pulses preferably lie in the middle between two s pulses. The pulses of the pulse train $h_1+h_5+\ldots$ always appear when half the digit period of the first binary digit of each tetrade has passed.

A somewhat different embodiment of this switching device is shown in Figure 4.1. Here a pulse train $s_1+s_5+\ldots$ which coincides precisely in time with the first synchronizing pulse s of each first binary digit in a tetrade, is used to reset the carry flip-flop 45 of the correction adder and to transfer the tetrade carry into the carry flip-flop 48 of the main adder. The same construction of adder-substractor as is shown in Figure 4 for the main adder can then be used for the correction adder. This is represented by the And-circuits and Or-circuits 50, 51, 52, 53, 54 with the inputs 20, 21, 55, 56, 57, 58, 59, 60 in Figure 4.1. The signal $\ddot{u}_{nk}$ at the output of the Or-circuit 54, which produces the carry into the next order place, alone indicates clearly whether a carry into the next tetrade is to take place or not at the end of the last binary digit period of each tetrade. The signal $\ddot{u}_{n\,k}$ is applied to gate 61 which receives the same pulse train $s_1+s_5+\ldots$ and in the case of pulse coincidence switches on the carry flip-flop 48 of the main adder.

The logical circuit which corresponds to the term $S_1 \cdot S_2+S_1 \cdot S_3+\ddot{u}_{n-1}$ was referred to above as a correction decider. A time must still be laid down at which this decision has to take place. In the example, the shift register has four places; consequently the binary digits S_1 to S_4 of the sum tetrade are available in the four flip-flops of the shift register the sum tetrade at the end of the tetrade and the carry into the next tetrade in the case of $\ddot{u}_n$ in the main adder. The least significant binary digit S_4 is, however, the same both corrected and uncorrected, because only O is added or subtracted. This least significant binary digit is therefore not required for the correction descision so that it may be allowed to enter the main storage device before the correction decision place. Thus the shift registers may be constructed with only three places.

It is even possible to reduce the number of places in the shift register to two. During the period of the fourth binary digit of the tetrade, S_1 appears at the output of the main adder, S_2 at the flip-flop 63 and S_3 at the flip-flop 64 of the shift register 7. S_3 would only be fed into the main storage device in this form with the synchronizing pulse s at the end of the binary digit period. The correction decision should therefore be carried out previously and the correct binary digit S_3 (corrected or uncorrected) should be supplied to the store. A pulse h_4, which comes before the synchronizing pulse s terminating the tetrade, may then be used. This pulse appears in the last binary digit period of each tetrade, preferably mid-way in time between two synchronizing pulses s. The synchronizing pulse s following h_4 must find the switching conditions due to h_4 already established, while h_4 must influence the switching conditions established by the preceding synchronizing pulse. If correction is necessary, then this pulse h_4 switches on a flip-flop 65 which effects a control in such a manner that the digits leaving the shift register 12 pass into the main storage device. If this flip-flop is not switched on, then the contents of the shift register 7 pass into the main store.

The control of this selection is effected, in accordance with the logical term

$$65 \cdot 67+\overline{66} \cdot 68,$$

wherein 66 and $\overline{66}$ represent the state of flip-flop 65; 67 the state of flip-flop 69 of the shift register 12, and 68 the state of flip-flop 61 of the shift register 7,

by two two-input And-circuits 70 and 71 and one two-input Or-circuit 72. A pulse h_3 which appears in the middle of the third binary digit period of each tetrade resets flip-flop 65 again after the corrected or uncorrected binary digits S_3, S_2 and S_1 of the sum tetrade have entered the store.

Figure 4.2 shows another embodiment of the control circuit for the flip-flop 65. The correction decider K_c issues a pulse h_1 to switch the flip-flop 65 to L when correction has to be effected, and the correction decision $\overline{K_c}$ inverted by a negator 70, switches the flip-flop 65 to O by means of pulse h_4 when no correction has to be effected. For example, if no correction is to be made several times in succession, then a pulse is constantly applied to the same side of the flip-flop 65 and this flip-flop remains in its original position. In the case of three-place shift registers, the selection of the correct sum tetrade digit may also be carried out in such a manner that the contents of the shift register 7 always enters the main storage device but that, when a correction has to be made, the contents of

the shift register 12 are transferred, by means of pulse h_1, into the shift register 7, for example through gate circuits.

The arrangement shown in Figure 1 may be simplified as shown in Figure 5. Again two tetrades $\underline{x_1}$ and $\underline{x_2}$ have to be added or subtracted. Figure 5 shows how the two terms are supplied from two cyclic stores 1 and 2 into the adder-subtractor 3, the augend to the added input 4 and the addend to the adder input 5. For subtraction, the minuend runs to input 4 and the subtrahend to input 5. The result leaving the adder at output 6 is conveyed to the shift register or the delay line 7. The output from the shift register 7 is conveyed on the one hand direct and on the other hand through the correction adder 8 to the selection circuit 14. The correction decider 73 is influenced by the contents of the shift register 7 and in turn causes the selection of the appropriate line in the selection circuit 74. The adder-subtractors 3 and 8 are of pure binary design, that is to say they have two inputs and one output. The shift register 7 may be composed of bistable flip-flop circuits which are stepped on by clock pulses. The selector 74 consists of two And-circuits brought together at the output side to form an Or-circuit The correction decider 73 is generally formed by an And-circuit and an Or-circuit to deliver the correction signal, the direct signal opening one path and its inversion the other. The sum enters the register 1 having been advanced by as many binary places as it is delayed by the delay line 7 so that the contents of the store are not displaced in relation to a definite starting position.

Figure 6 shows the arrangement in more detail. A shift register consisting of two bistable flip-flop circuits 88 and 92 is selected as a delay line, and for the control are used intermediate pulses h which appear, in time, between the pulses designated by s, which initiate the binary place periods. In a somewhat modified construction, these intermediate pulses h could be avoided, but then at least three bistable flip-flop circuits are needed in the delay line as intermediate stores. In Figure 6 again, And-circuits are designated by empty circles, Or-circuits by shaded circles, the dot and each circle representing the output of each circuit. The inverting elements are designated by N, the pulse gates by G. The pulse gates G not only have the switching pulse input but also a pulse input for the synchronizing pulse "s" or for the intermediate pulse "h". One of the last mentioned pulses in conjunction with a switch pulse L at the switching pulse input provided at the pulse output of a pulse gate G a pulse for changing over a bistable flip-flop stage. In the bistable flip-flop stages, the pulse inputs are designated by arrows, the switch outputs for signals of longer duration are not designated.

Figure 6 likewise shows the two store tracks 1 and 2. Track 1 is shortened by two binary places compared with track 1. The store outputs convey the signals representing the digits to the adder inputs 4 and 5. The inverted signals $\overline{4}$ and $\overline{5}$ of the store outputs are likewise supplied to the main adder. The inverted signals are produced by the inverting elements 116 and 117. The first binary adder, that is to say the main adder for the serial addition of the binary digits together with the associated carry delay is formed in known manner by:—

1. And-circuits 75, 76, 77 and 78 and Or-circuits 81 for forming the binary sum output 85;

2. And-circuit 79 and pulse gate 125 for switching on the flip-flop circuit 83 for the carry delay. In these switching operations, the known switching method is used according to which the transit time of the switching signals at the pulse instant always leaves the previous state still effective.

3. And-circuit 80 and pulse gate 82 for switching off the carry flip-flop circuits 83; and

4. Flip-flop circuit 83 to delay the carry.

The shift line which is operated by the synchronizing pulse train s which initiates each binary digit period, and which steps on the contents by one place, is formed in known manner by:—

1. Negator 127 for forming the inverted binary sum 85;

2. Pulse gates 86, 87, 90 and 91; and

3. Bistable circuits 88 and 92.

A simplified form of adder may be used for the correction adder 8. The binary sum is formed in the same manner as in the main adder 3 by the And-circuit 95, 96, 97 and 98 and the Or-circuit 103. The output 93 $\overline{93}$ from the delay line 7 on the one hand and the correction tetrade 94, $\overline{94}$ on the other hand are supplied to the correction adder 8.

The correction tetrade 94 or its inverted value $\overline{94}$ is a rectangular pulse voltage wave of half the digit frequency because the 4-unit sequence corresponding to the decimal digit "six" corresponds to the sequence OLLO, OLLO . . . The reversing points of the voltage wave 94 should therefore be placed in such a manner that it assumes the value L during the two middle binary digit periods of each tetrade. The carry circuit comprising an And-circuit 99 and the pulse gate 100, to the pulse input of which the synchronizing pulse s is applied, is also like that of the main adder 3. The switching off of the

flip-flop circuit 101 to delay the carry is considerably simplified, however, in that a pulse train $h_1+h_5+\ldots$ with pulses appearing in the middle of each first binary digit period of the tetrade always effects the switching off. The carry flip-flop circuit can now be switched on in one of the two middle binary digit places of the tetrade because only here does the "six" contain signals corresponding to the binary L. In this case, however, this flip-flop circuit must always remain switched on precisely until the end of the tetrade period because a carry occurring in the second binary digit place is sure to produce, in the third place, a carry into the fourth place, because the carry of the second place together with the L in the third place produces a fresh carry. On the other hand, the correction adder 8 cannot be used here to delay the carry into the next tetrade. The L of the decimal carry has to be delayed in the main adder or supplied to the main adder. A decimal carry always appears when a correction has to be made, and a bistable flip-flop circuit 109 is switched on. The supplying of the decimal carry to the main adder is shown in the drawing in such a manner that the signal 110 supplied by the flip-flop circuit 89 is applied to the switching input of a pulse gate 115, to the pulse input of which is supplied the pulse train $h_1+h_5+\ldots$

The pulse gate 115 switches on the carry flip-flop circuit 83 of the main adder 3. The correction decision is reached by a circuit which is composed in accordance with the following logical expression:—

$$116+85\,.\,93+85\,.\,29=116+85\,.\,(93+89).$$

In Figure 6, this expression is formed by the Or-circuit 112 and the And-circuits 113 and 114. The switching on of the flip-flop circuit 109, which is switched on whenever the corrected tetrade has to be selected, is effected with the sequence $h_4+h_8+\ldots$ which delivers a pulse in the middle of each fourth binary digit period of the tetrades. The switching off is effected one binary digit period earlier by the pulse train $h_3+h_7+\ldots$ The pulse train $h_4+h_8+\ldots$ may be the differentiated downwards going flank of the rectangular switching voltage wave 94 if the L of this wave extends from h_2 to h_4 which may be the case. In the correction decision, the term 25 . (33+29 allows for the appearance of a pseudo-decimal and 126 for the case when no pseudo-decimal appears but a carry into the next tetrade. In the latter case, the carry is always introduced only the fourth digit. With the synchronizing pulses s_1 the first binary digit of the tetrade is taken from the storage device and supplied to the inputs of the calculating device. With the synchronizing pulses s_4, the fourth binary digit reaches the calculating device. The first binary digit, after having passed through the flip-flop circuits 88 and 92 in the second and third digit periods, has re-entered the main store. During the passage of this first digit into the storage device at s_4, flip-flop circuit 109 was switched off by the pulse train $h_3+h_7+\ldots$ The first digit is the same, however, whether corrected or uncorrected, so that it is immaterial which of the two lines 93 or 104 is selected. At the time of the correction decision, the second binary digit of the sum tetrade is at 93, the third at 89 and the fourth at 85. These are the three binary digits which are decisive in indicating the pseudo-decimals.

Figure 7 shows that part of the correction device which varies in into design for addition and subtraction respectively. In the main adder 3, the And-circuits 79, 80 for processing the carry are extended by a third input signal 117. The signal 117 is always an L in the case of addition. During subtraction, another switching on and off means is necessary for the carry and is produced by the And-circuits 118 and 119 to which the control signal 120 is applied which only assumes a value corresponding to L during subtraction. The possibility of switching on and off for addition or subtraction is controlled by the Or-circuits 121 and 122. In the correction adder 8, the And-circuit 99 for the switching on of the carry is extended by the third input signal 117. In subtraction, another another means of switching on the carry is necessary and is produced by the And-circuit 123 to which the control signal 120 is applied. The two possibilities of switching on are afforded through the Or-circuit 124. Both adders, the main adder and the correction adder, are switched over in the same manner and through the same line to carry out the addition or subtraction operations.

The bistable flip-flop stages may be realised by known valve flip-flop stages or by the flip-flop circuit each comprising two transistors. The negaters are inverting circuits. The And-circuits and Or-circuits may be diode switching circuits. The known triode gates with double feed at the grid or additional feed through a cathode resistance, or gates with double control valves, or even diode coincidence circuits may be used as pulse gates.

WHAT WE CLAIM IS:—

1. A serial calculating device for the addition or subtraction of two decimal numbers the individual digits of which are coded in a binary four-digit code, which calculating device comprises a main adder-subtractor to which the individual four-digit (tetrades) of the two decimal numbers are supplied in succession and in serial mode, a correction adder-subtractor which receives the output from the said main adder-subtractor and the required correction tetrade to produce their algebraic sum, the output from the said main adder-subtractor being added into or sub-

tracted from the correction adder-subtractor according to whether the said two decimal numbers are being or subtracted respectively, and a selector unit which, depending on whether correction was necessary or not, selects for further processing the tetrade issued by the main adder-subtractor or the tetrade issued by the correction adder-subtractor.

2. A calculating device as claimed in Claim 1, further comprising a shift register to which the sum tetrade formed in the main adder-subtractor is supplied, another shift register to which the tetrade formed in the correction adder-subtractor is supplied, and a correction decider which is connected to the shift register supplied from the main adder-subtractor and the output of which influences the said selector unit to select for further processing either the contents of the shift register supplied by the main adder-subtractor or of the shift register supplied by the correction adder-subtractor.

3. A calculating device as claimed in Claim 1, further comprising a shift register to which the sum tetrade formed in the main adder-subtractor is supplied and which is connected to the correction adder-subtractor to supply to the latter the sum tetrade found in the main adder-subtractor, a selector unit connected to the output of the said shift register as well as to the output of the correction adder-subtractor, and a correction decider which has its input connected to the said shift register and which influences by its outputs the said selector unit to select the sum tetrade or the correct sum tetrade.

4. A calculating device as claimed in Claim 1 and 2 wherein the main adder-subtractor and the correction adder-subtractor are switched over jointly to addition or subtraction through the same control lines.

5. A calculating device as claimed in Claim 2 or 4, wherein the selection of the corrected tetrade is effected in such a manner that the said selector unit blocks the output from the shift register that is connected to the main adder-subtractor and opens the output from the shift register that is connected to the correction adder-subtractor.

6. A calculating device as claimed in Claim 2 or 4 wherein the selection of the correction or uncorrected sum tetrade is effected by the said selector unit in such a manner that only the contents of one shift register are issued for further processing and, when required, the contents of the other shift register are previously transferred to the first named shift register.

7. A calculating device as claimed in Claim 2, wherein the selective switching over of the main adder-subtractor to addition or subtraction is effected by two control signals (20 and 21) of which one is supplied to two And-circuits (22, 24) and the other to two And-circuits (23, 25), which And-circuits control the switching on and off of the flip-flop (19) which forms the carry into the next binary place in such a manner that during addition the conjunction (22) of the two binary digits to be added and of the signal (20) forming the instruction for addition causes the switching on the carry flip-flop (19) and the carry flip-flop is only switched off again by the conjunction (24) of the two inverted binary digits to be added and of the signal (20), whereas during subtraction, the carry flip-flop (19) is switched on by the conjunction (23) of the inverted binary digit of the minuend, of the binary digit of the subtrahend and of the signal (21) indicating subtraction, and the carry flip-flop (19) is switch back to O by the conjunction (25) of the binary digit of the minuend, the inverted binary digit of the subtrahend and the signal (21) indicating the subtraction.

8. A calculating device as claimed in Claim 2, wherein the selective switching over of the adder-subtractors (3, 8) to addition or subtraction is effected through two signals (20 and 21) of which signal (20) is supplied to And-circuits (39 and 40) and signal (21) is supplied to And-circuits (42 and 43) which And-circuits control the switching on and off of flip-flop (48) forming the carry into the next binary place in such a manner that, when the logical circuit

$$a \cdot b \cdot 20 + \ddot{u}_{n-1} \cdot S_1 \cdot 20 + \bar{a} \cdot b \cdot 21 + \bar{S} \cdot \ddot{u}_{n-1} \cdot 21$$

(39, 40, 41, 42, 43) with a as addend or minuend, $\bar{a}$ for example as inverted addend, b as subtrahend or augend, $\ddot{u}_{n-1}$ as carry from the sum of the two previous binary digits, S_1 as binary partial sum of the two operand digits, 20 as the signal indicating the addition, and 21 as the signal indicating the subtraction, delivers a signal corresponding to L, a carry is sent into the next place, whereas no carry is effected when the signal O is delivered.

9. A calculating device as claimed in Claims 2, 7 and 8, wherein no carry from a preceding tetrade is processed in the correction adder (8), but that such tetrade carry is supplied to the main adder (3).

10. A calculating device as claimed in Claims 2, 7, 8 and 9, wherein a pulse ($h_1 + h_2 + \ldots$) which appears substantially in the middle of each first binary place period of a tetrade, resets the carry flip-flop (45) associated with the correction adder (8), and wherein the same pulse then switches on the carry flip-flop (48) of the main adder (3), for

example through a controlled pulse gate (46).

11. A calculating device as claimed in Claim 2, 7, 8 and 9, wherein a pulse train ($s_1+s_5+\ldots$) which coincides in time with the synchronizing pulse (s) initiating the first binary digit of each tetrade, is used to cancel the tetrade carry in the carry flip-flop (45) of the correction adder (8) and to the transfer it to the carry flip-flop (48) of the main adder-subtractor (3).

12. A calculating device as claimed in Claims 2 and any one of the Claims 4 to 11, wherein the shift registers (7 and 12) each comprise two binary places and the least significant digit of the tetrade is caused to enter a storage device before the correction decision is made.

13. A calculating device as claimed in Claim 2 and 4 to 12, wherein a pulse (h_4) which is situated in time in the last binary digit period of each tetrade initiates the selection of the same tetrade or of the corrected tetrade.

14. A calculating device as claimed in Claims 2 and 4 to 13, wherein the instruction delivered by the logical circuit ($S_1 \cdot S_2+S_1 \cdot S_3+\ddot{u}_{n-1}=K_e$) as to whether correction is to be effected is held by a flip-flop (65) until the tetrade has been transferred to a storage device.

15. A calculating device as claimed in Claim 2 and 4 to 14, wherein a pulse (h_3) which appears during the third binary digit period of each tetrade resets the flip-flop (65) again.

16. A calculating device as claimed in Claims 2 and 4 to 15, wherein instruction resulting from the correction decision (K_e) is supplied to the "on" side of the flip-flop (65) and the inverted correction instruction ($\overline{K_e}$) is supplied to the "off" side of the flip-flop (65) in such a manner that an instruction corresponding to L in coincidence with a brief pulse switches the associated side of the flip-flop to L, the said brief pulse (h_4) occurring in the fourth binary digit period of the tetrade.

17. A calculating device as claimed in Claims 2 and 4 to 16, wherein the correction value corresponding to the binary Six is supplied to the correction adder (8) in the form of a non-controlled rectangular waveform (44 or $\overline{44}$) the positive going and the negative going flanks lie respectively at the end of the first and third binary digit period of each tetrade.

18. A calculating device as claimed in Claim 3, characterised in that, particularly with a coding of the decimal digits, by their binary numbers the switching off of the flip-flop circuit which delays the carry always takes place, uncontrolled by the digit course, only after the termination of the tetrade period.

19. A calculating device as claimed in Claims 3 and 18, wherein the main adder-subtractor (3) and the correction adder-subtractor (8) are switched over jointly to addition or subtraction through the same control lines.

20. A calculating device as claimed in Claims 3, 18 and 19, wherein the tetrade carry formed is always supplied to the main adder in such a manner that, whenever correction is necessary, the flip-flop circuit of the main adder, which delays the carry, is switch on during the period of the first binary digit of the tetrade.

21. A calculating device as claimed in Claims 3 and 18 to 20, wherein the shift register accommodates as many binary values as each decimal digit contains binary digits.

22. A calculating device as claimed in Claims 3 and 18 to 20, wherein the shift register accommodates fewer binary values than each decimal digit contains binary digits, particularly with 4-unit coding where the shift register delays at least two binary digits.

23. A calculating device as claimed in Claims 3 and 18 to 22, wherein the correction value corresponding to the binary "Six" is supplied to the correction adder (8) in the form of an uncontrolled rectangular waveform of half the binary digit frequency of the calculating device.

24. A calculating device as claimed in Claims 3 and 18 to 23, wherein the selection of the corrected or uncorrected tetrade begins only after the output of the first binary digit has been terminated.

25. A calculating device substantially as described with reference to and as illustrated in Figure 1 and 4 or modified in accordance to Figure 4.1 or Figure 4.2 or in Figures 5 and 6 or modified in accordance to Figure 7.

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5 SHEETS

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SHEET 1

FIG. 1

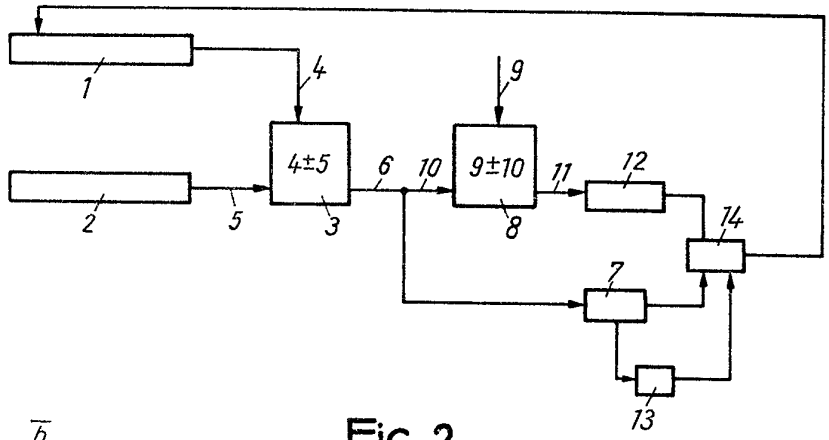


FIG. 2

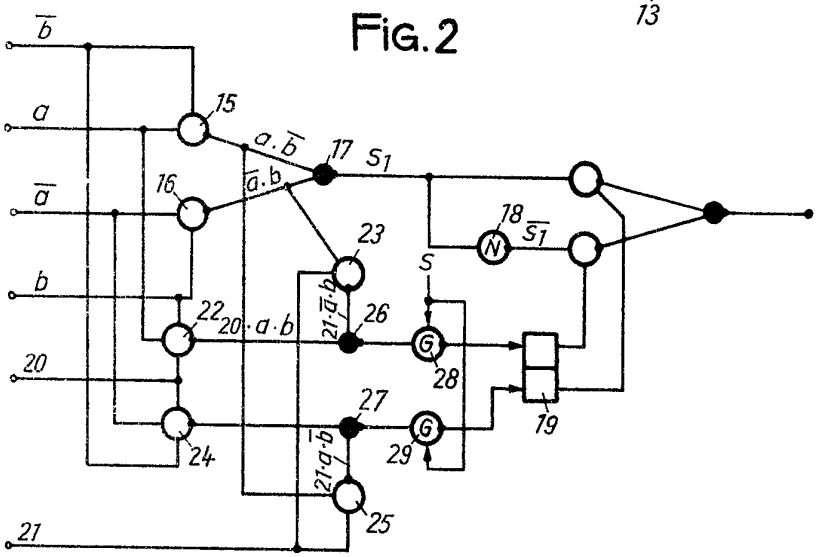


FIG. 3

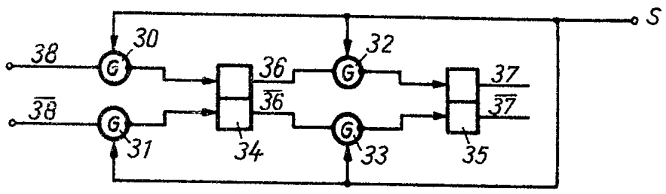
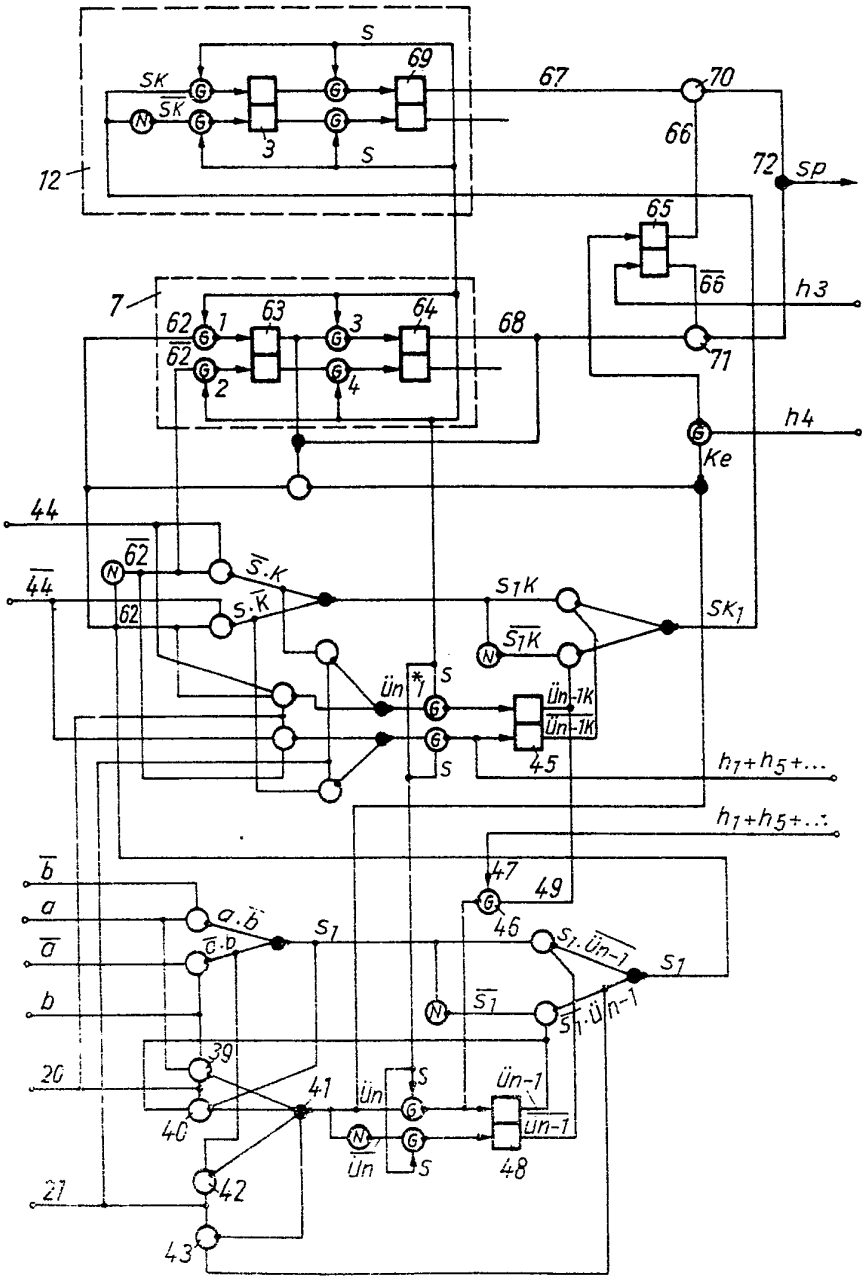


Fig.4


S
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SK
67
70
66
12
3
72
sp
65
7
62
63
64
68
h3
71
h4
Ke
44
S1K
SK1
Ün
45
h1+h5+...
47
49
46
S1
20
39
41
40
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48

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SHEETS 2 & 3

FIG. 4.1

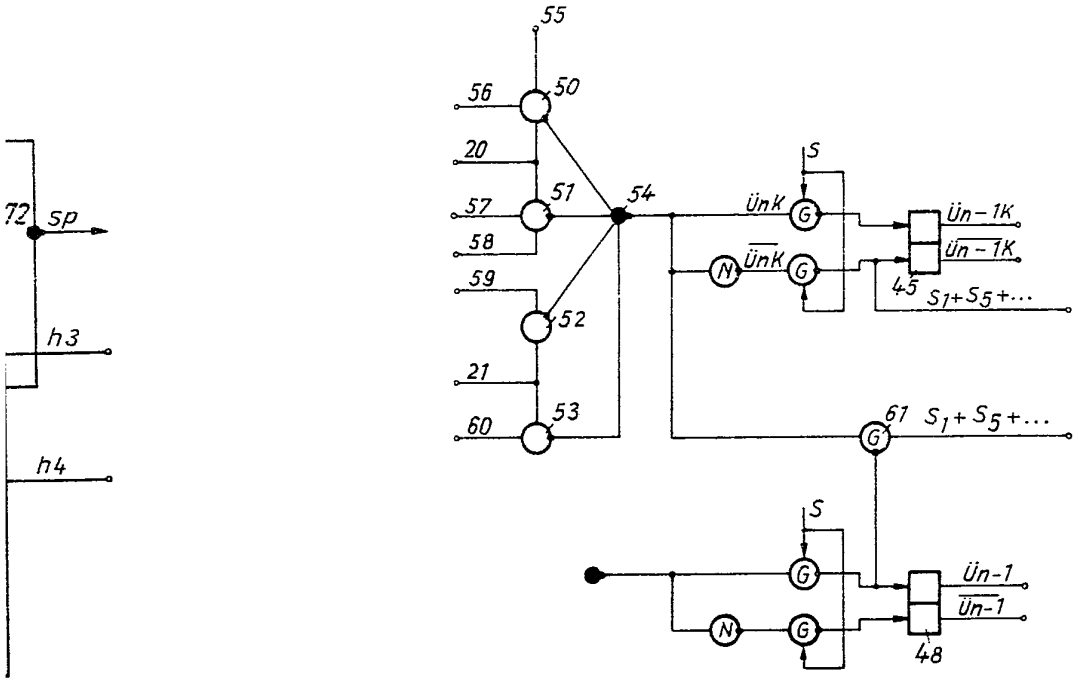


FIG. 4.2

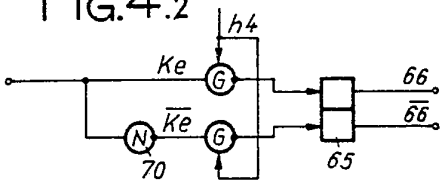


FIG. 8

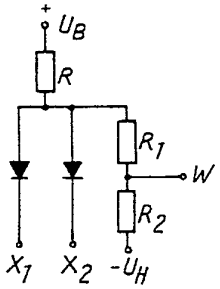
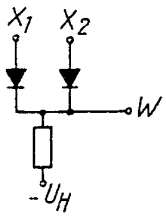


FIG. 9



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SHEETS 2 & 3

Fig.4

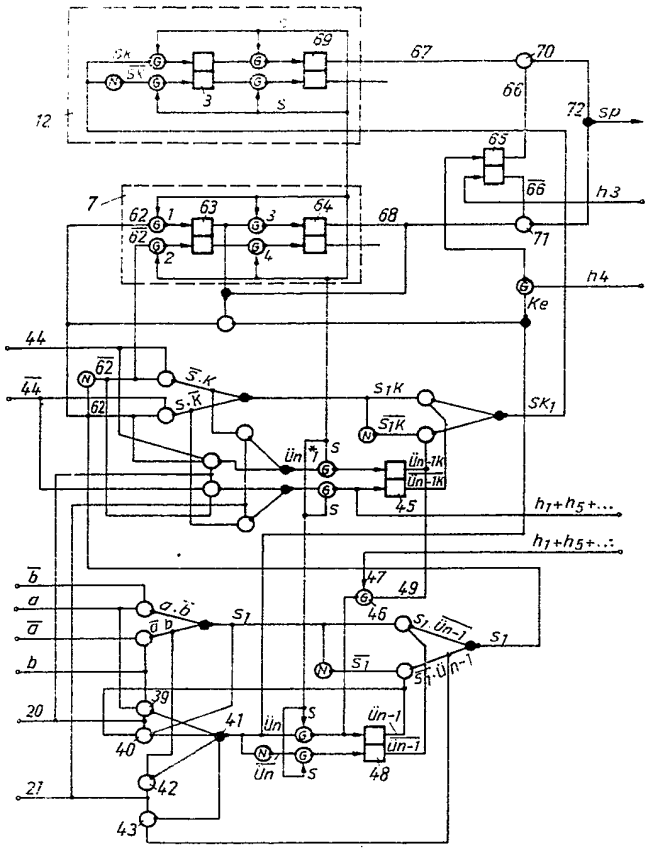


Fig.4 1

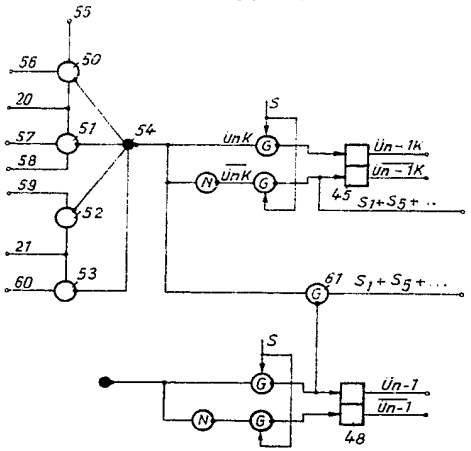


Fig.4.2

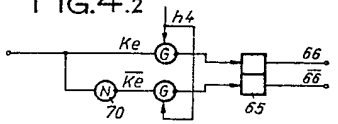


Fig.8

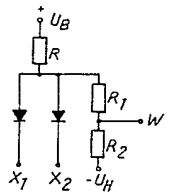


Fig.9

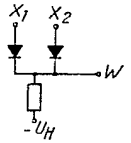
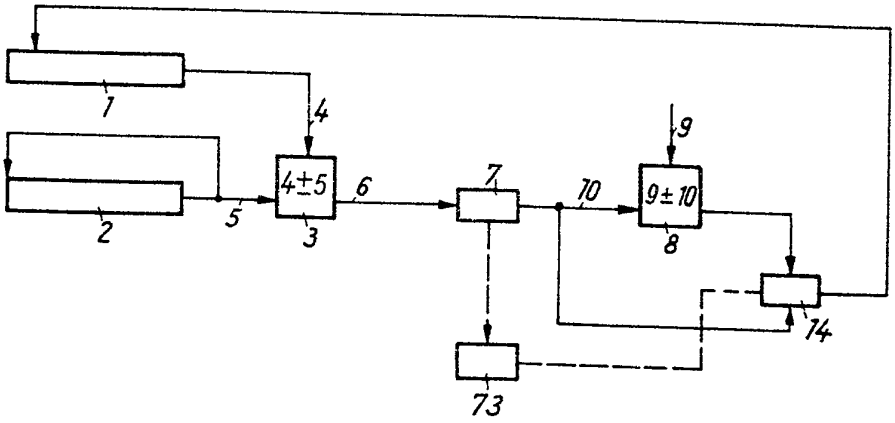


Fig.5


1
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10
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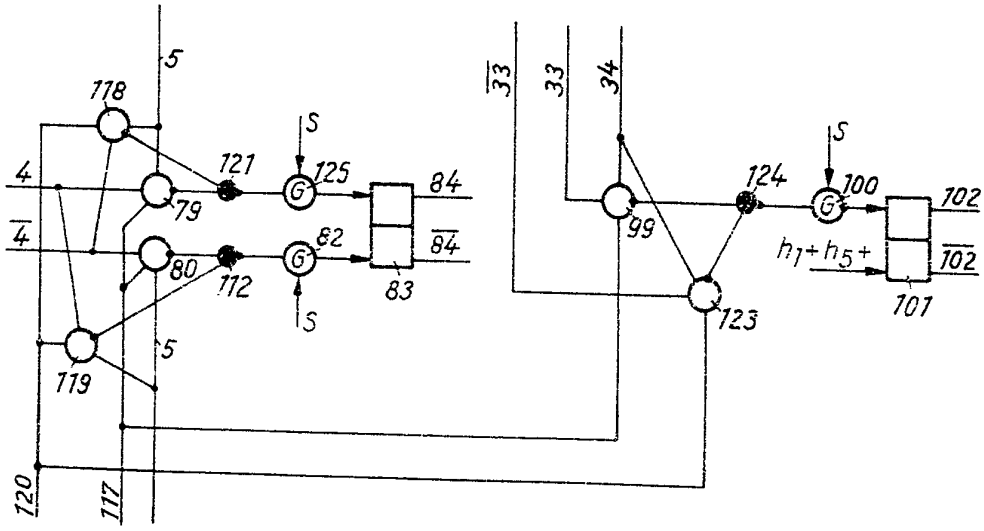
9±10
8
14
73

Fig.7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118
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79
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S
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112
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84
83
S
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120
117
33
33
34
99
124
S
100
G
102
102
101
123
h1+h5+

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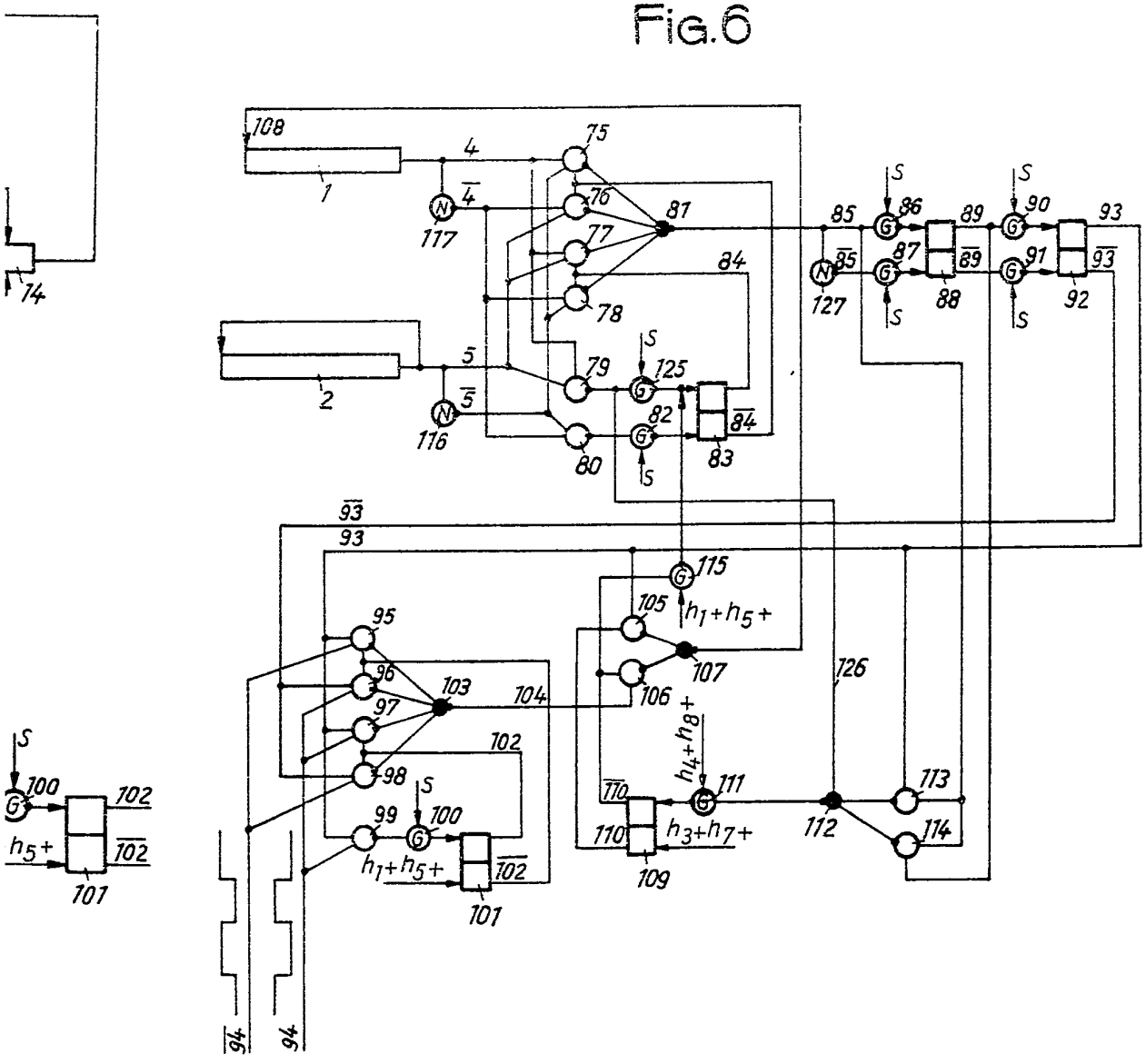
SHEETS 4 & 5

Fig.6



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SHEETS 4 & 5

Fig.5

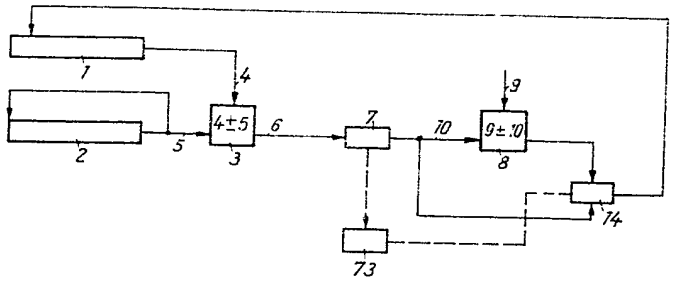

Fig.6

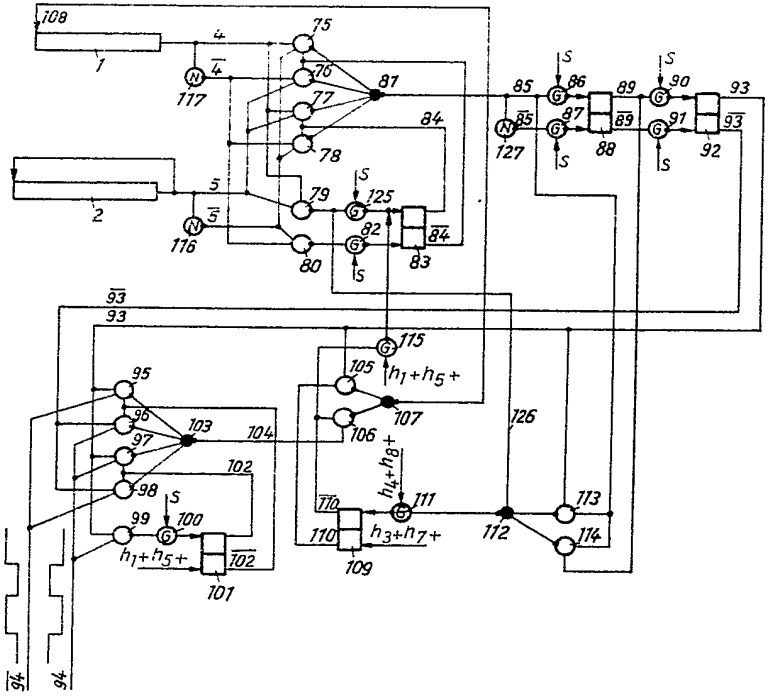

Fig.7